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Prior Art

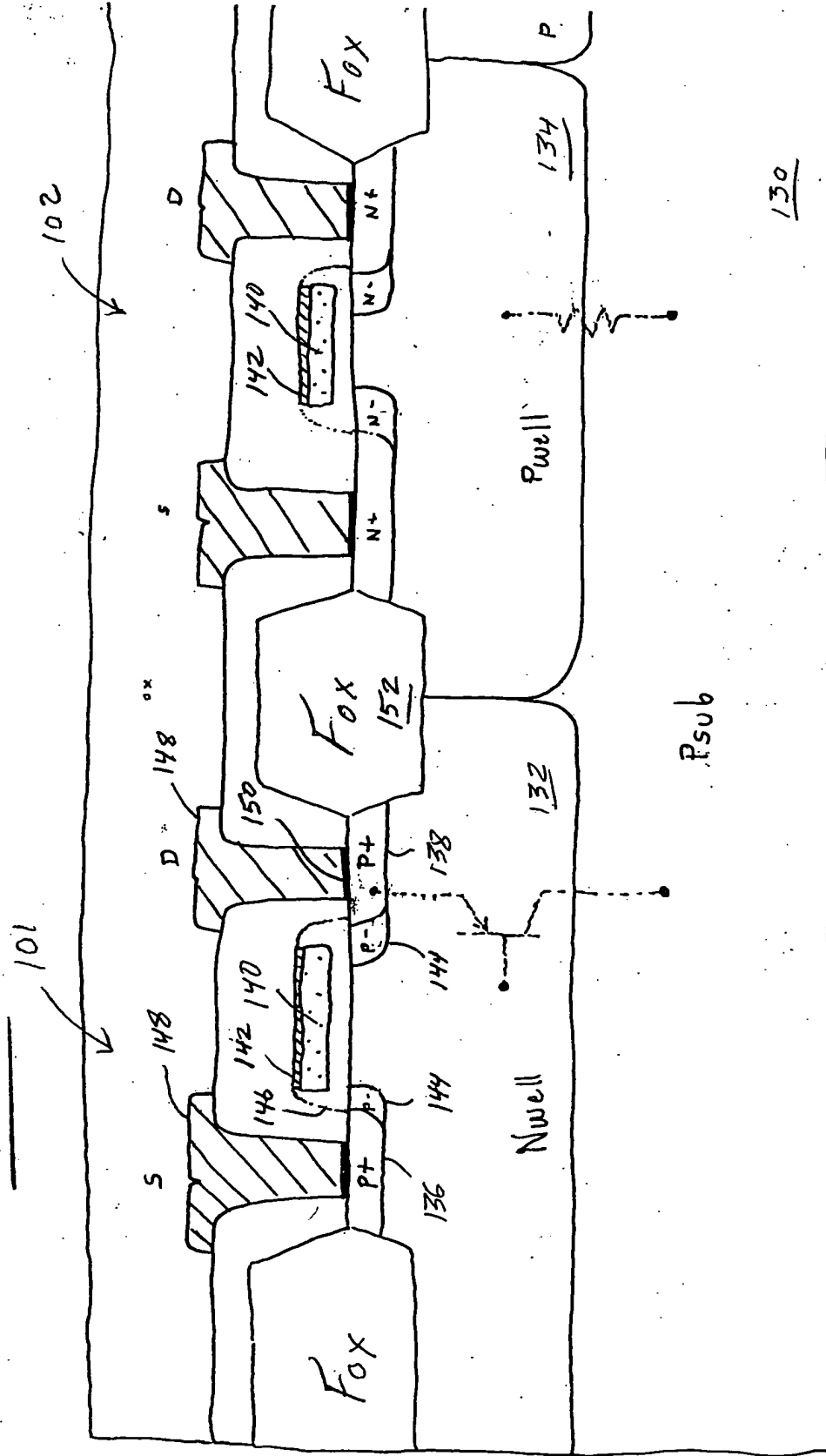


Fig. 1B

Prior Art

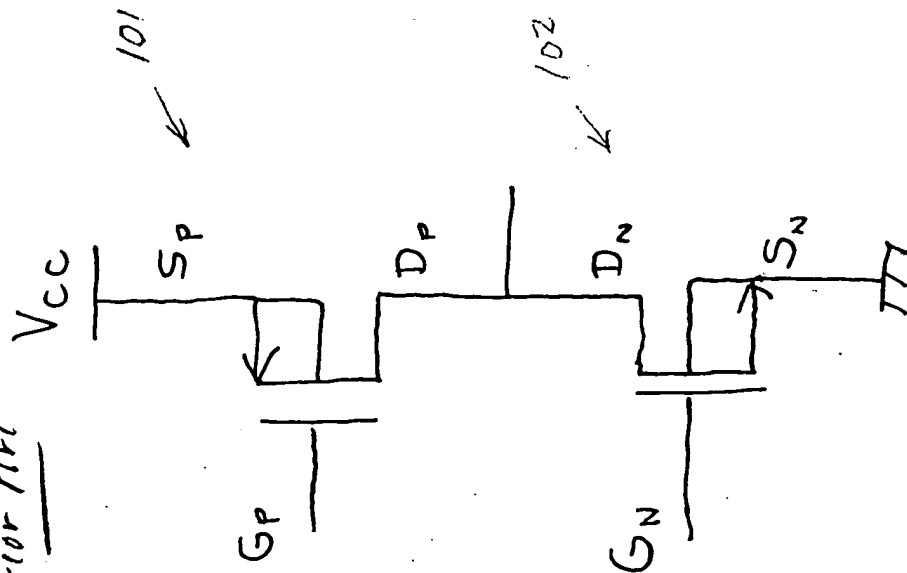


Fig. 1C

Prior Art

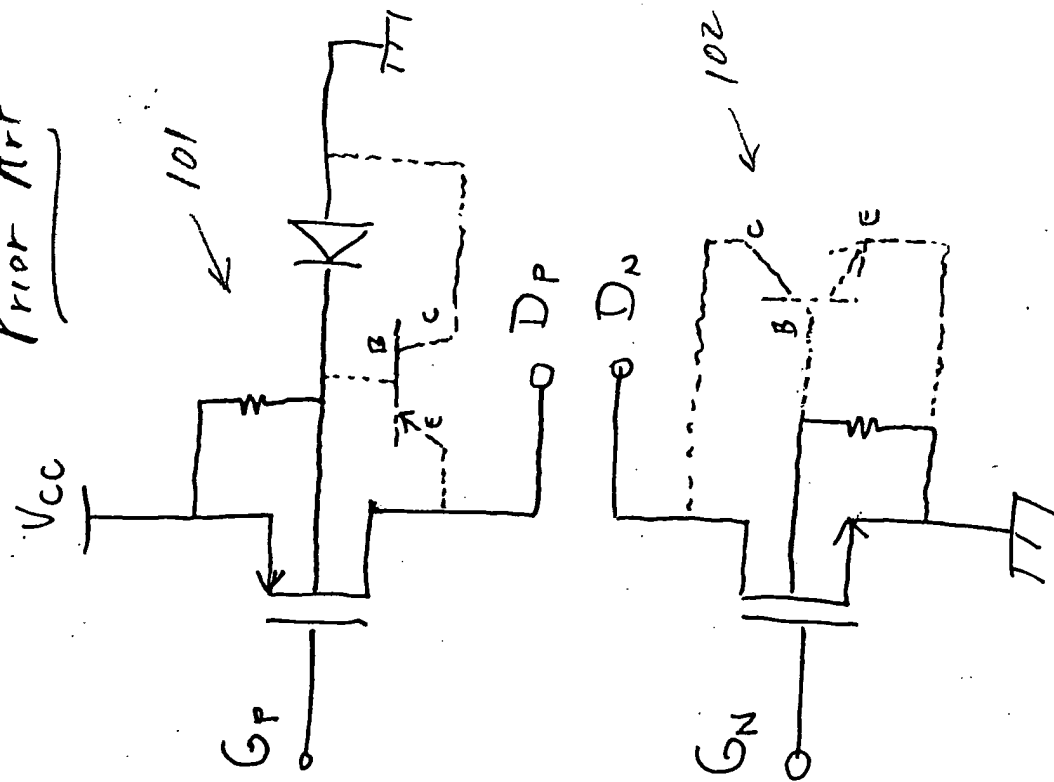


Fig. 2A

Prior Art

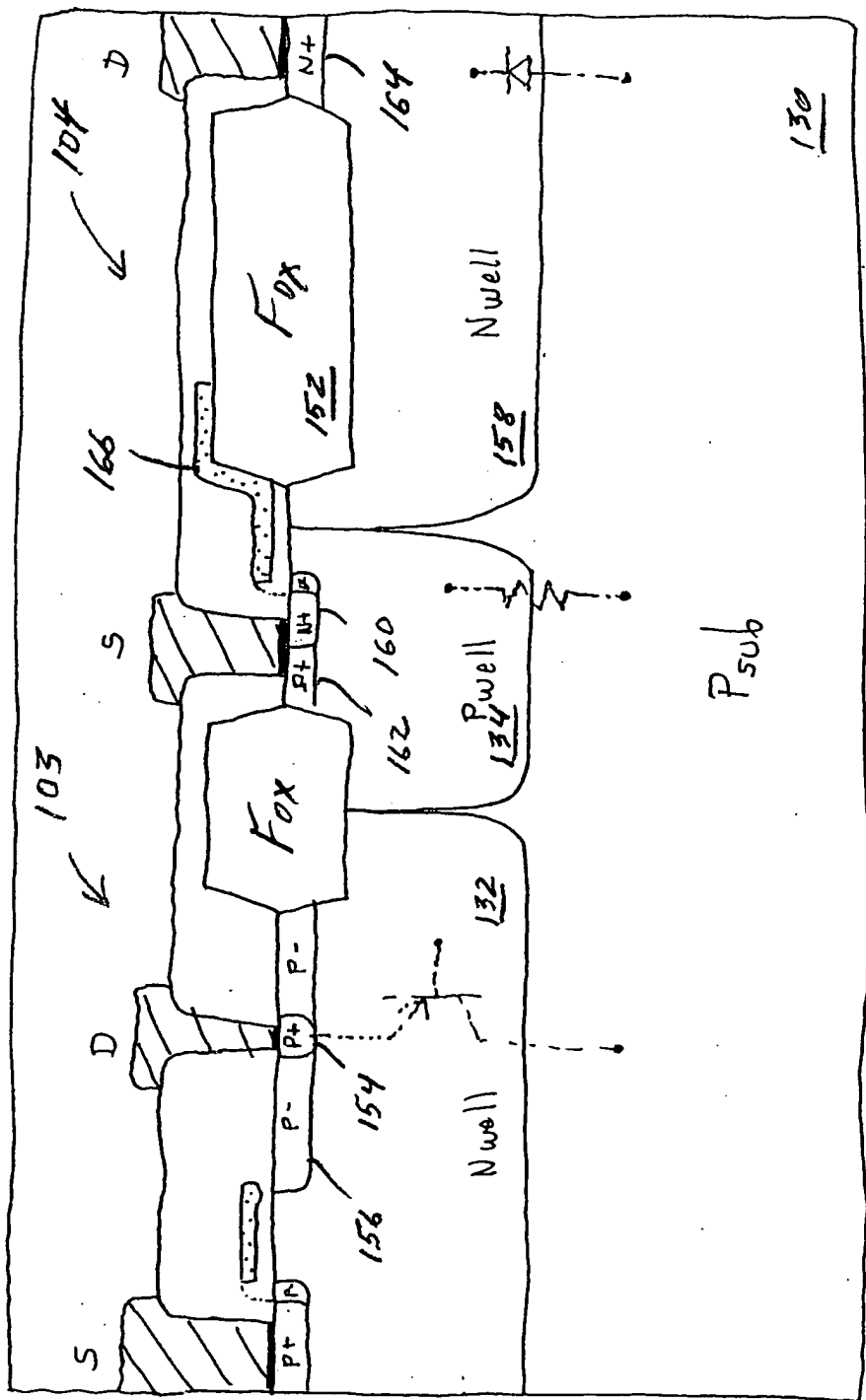
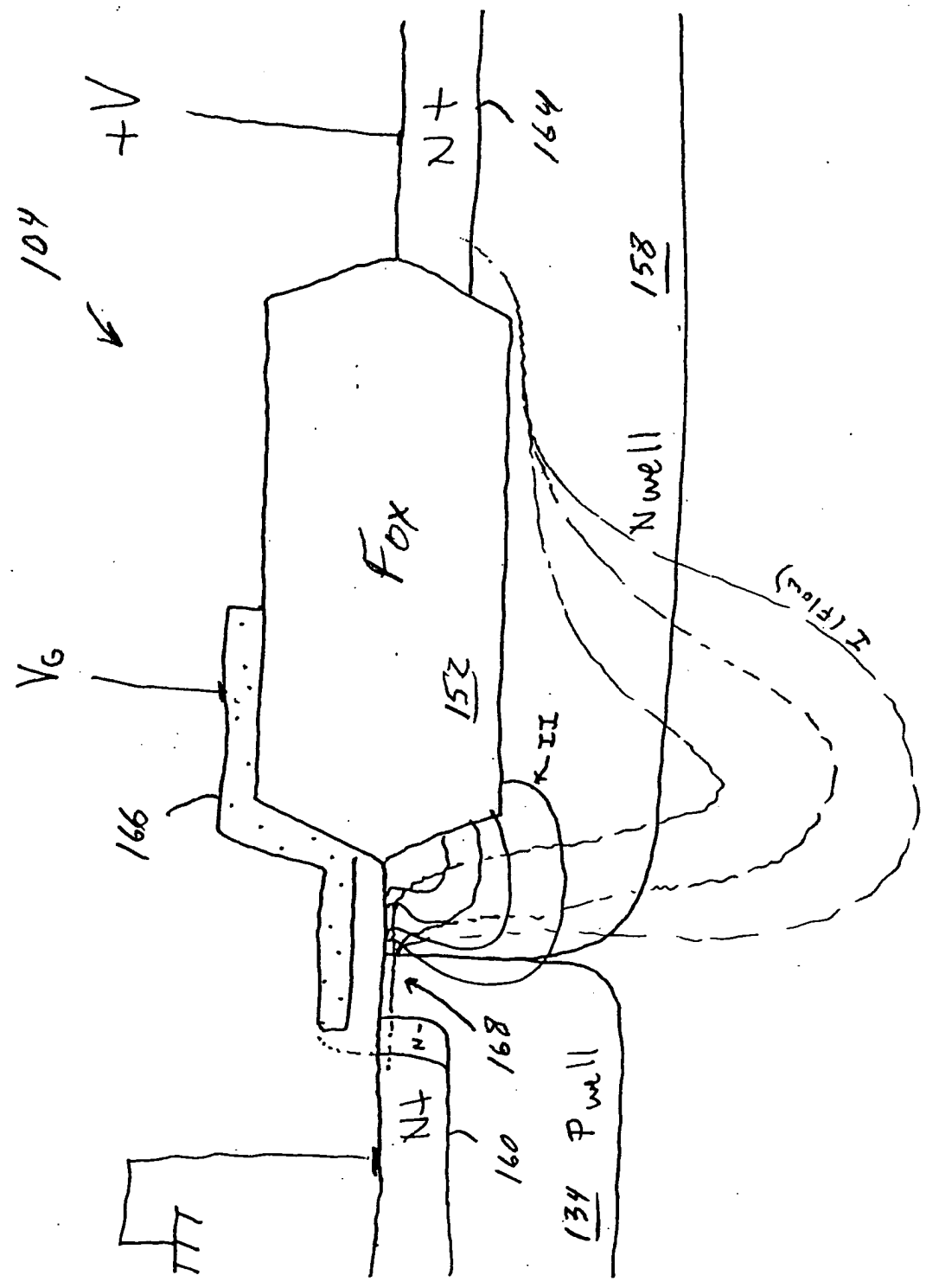


Fig. 2B

Prior Art



5/219

Fig 2C

Prior Art

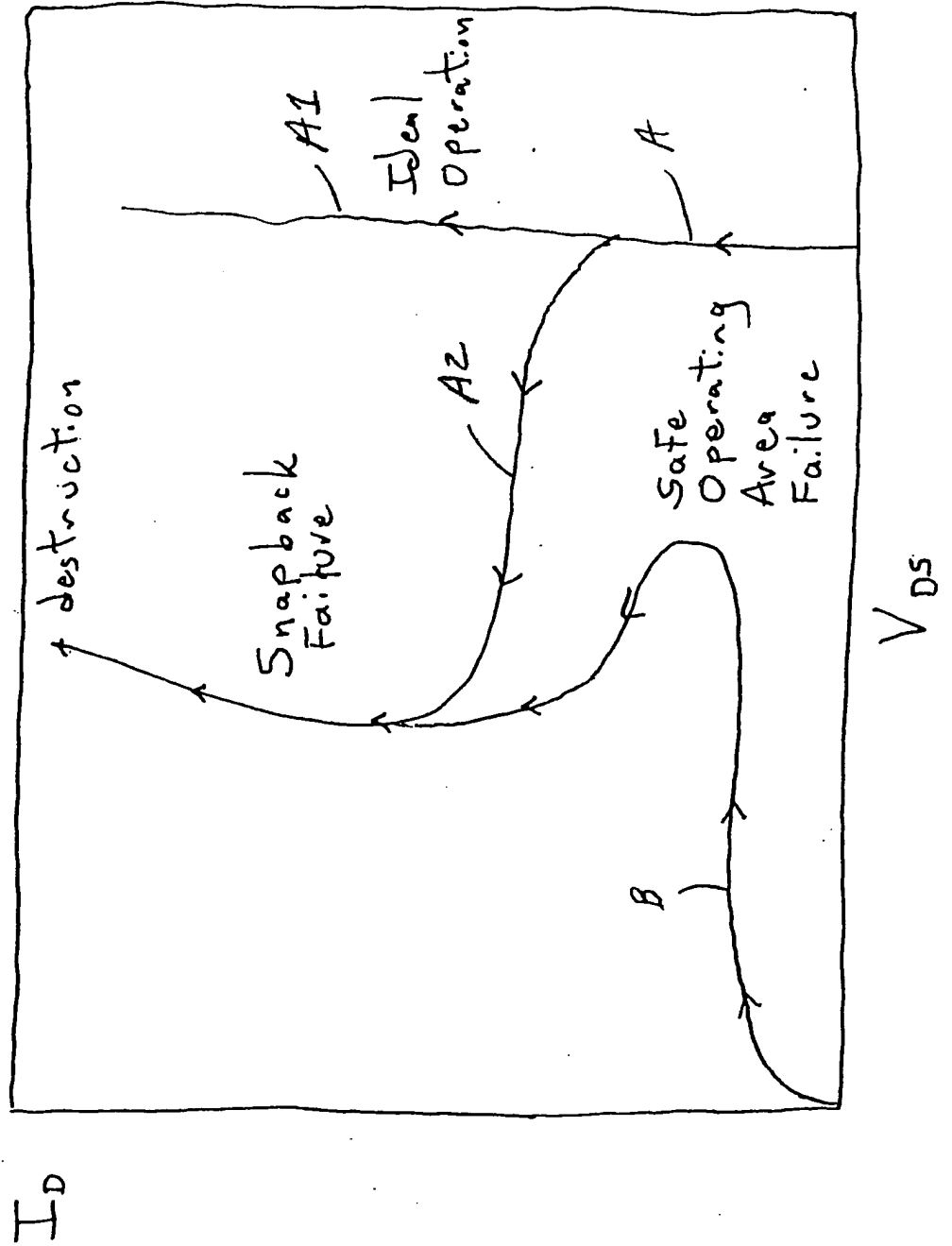
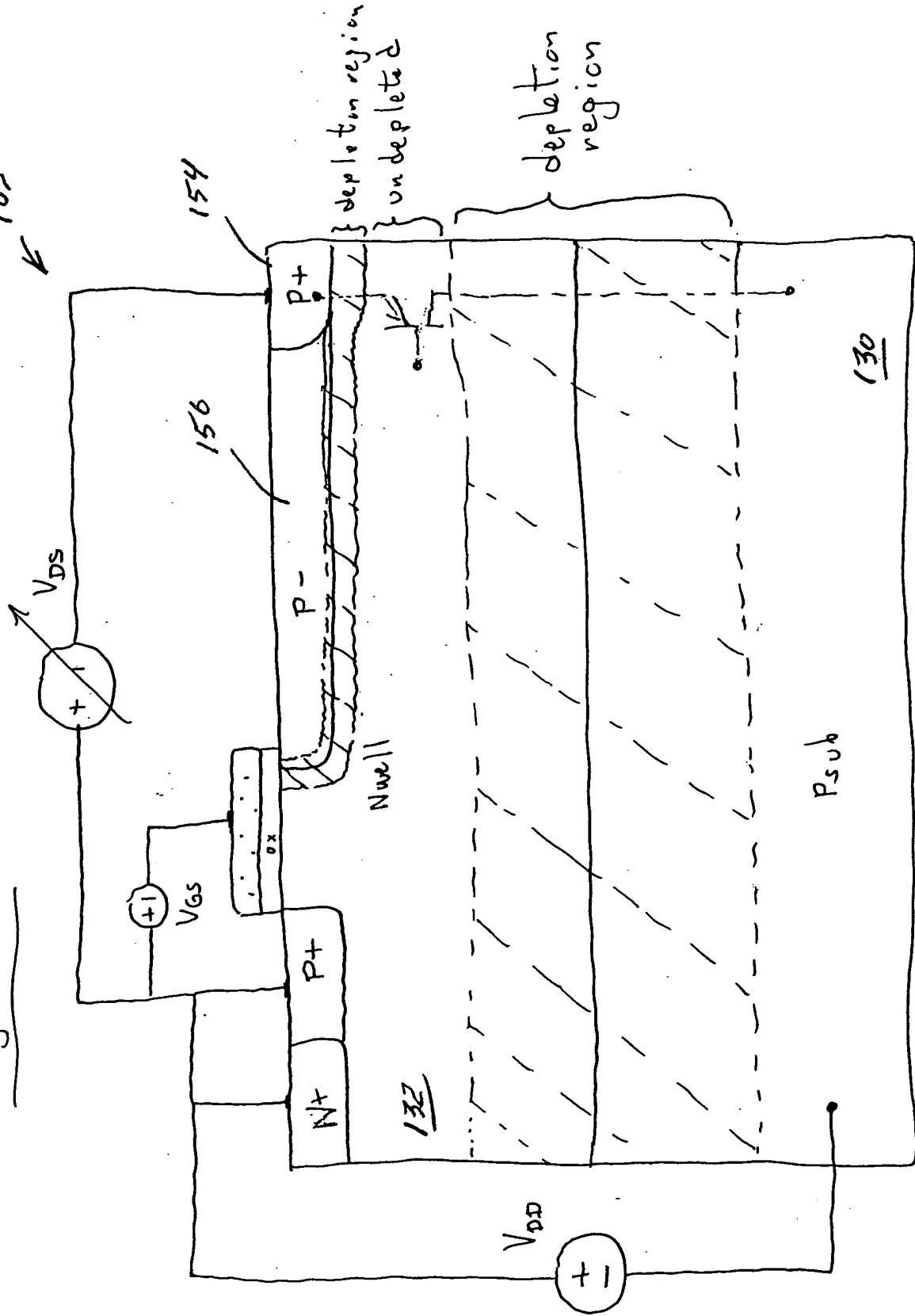
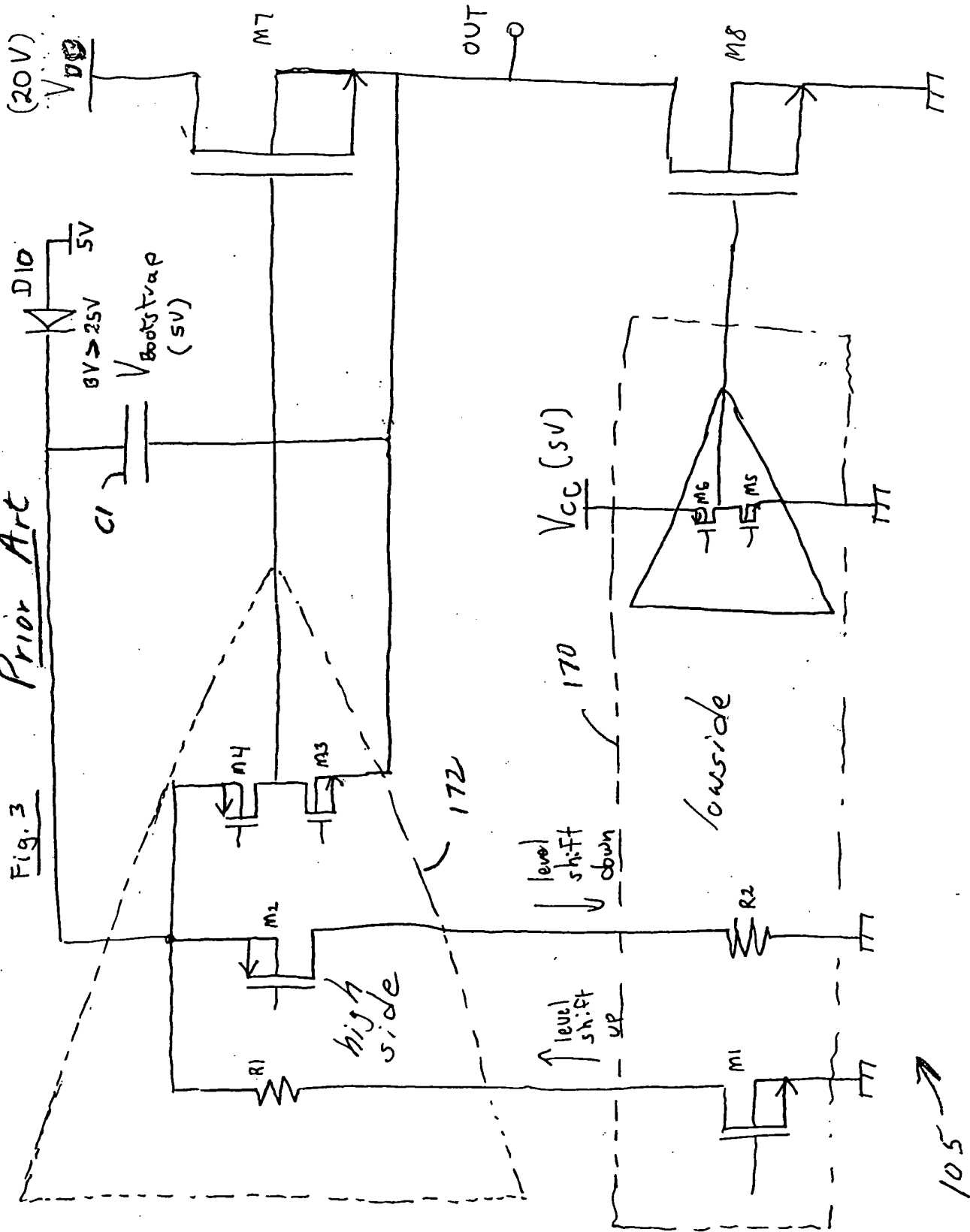


Fig. 2D Prior Art 103



7/219

Fig. 3 Prior Art



8/219

Fig. 4A

Prior Art

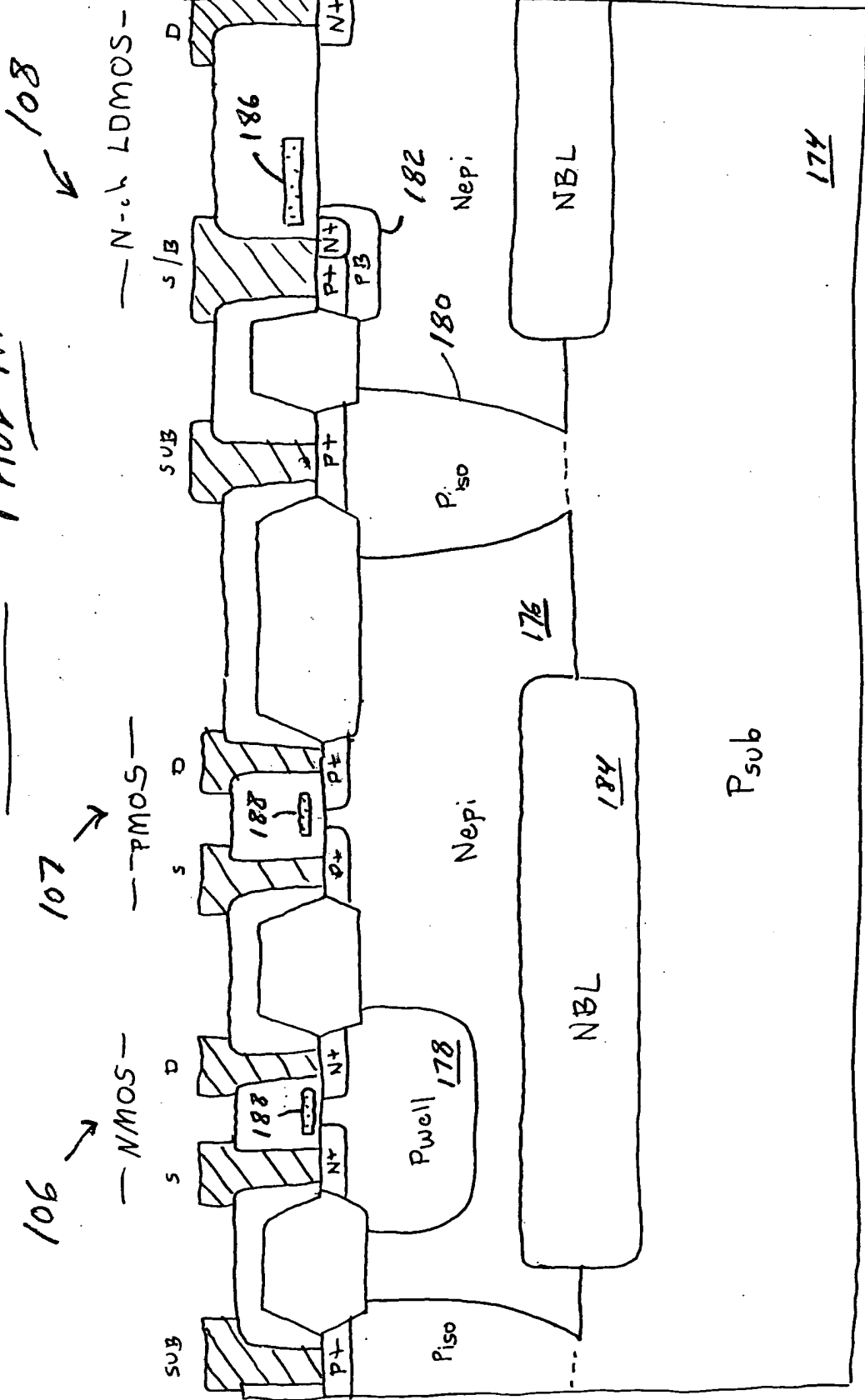
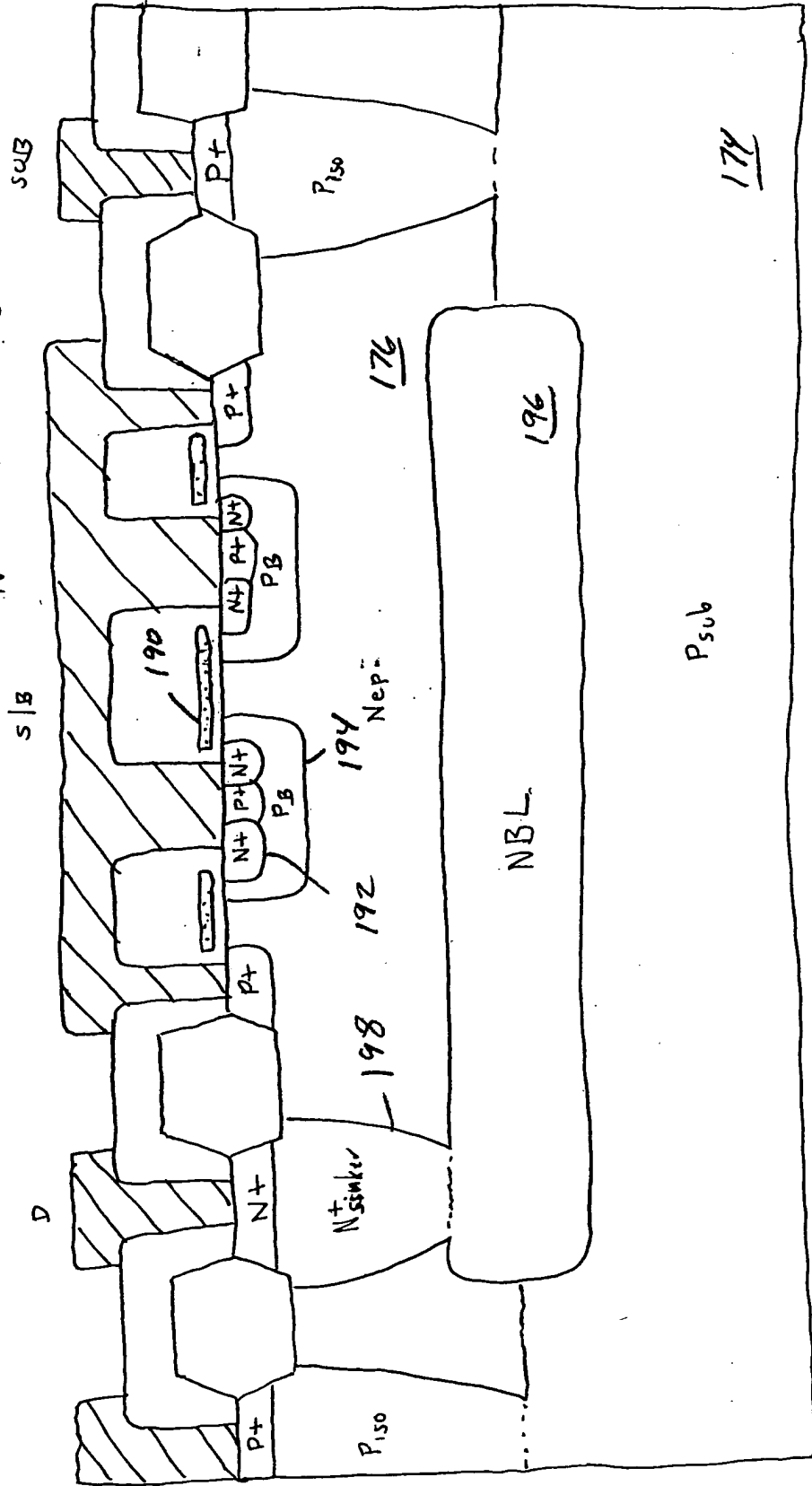


Fig. 4B

109

Prior Art

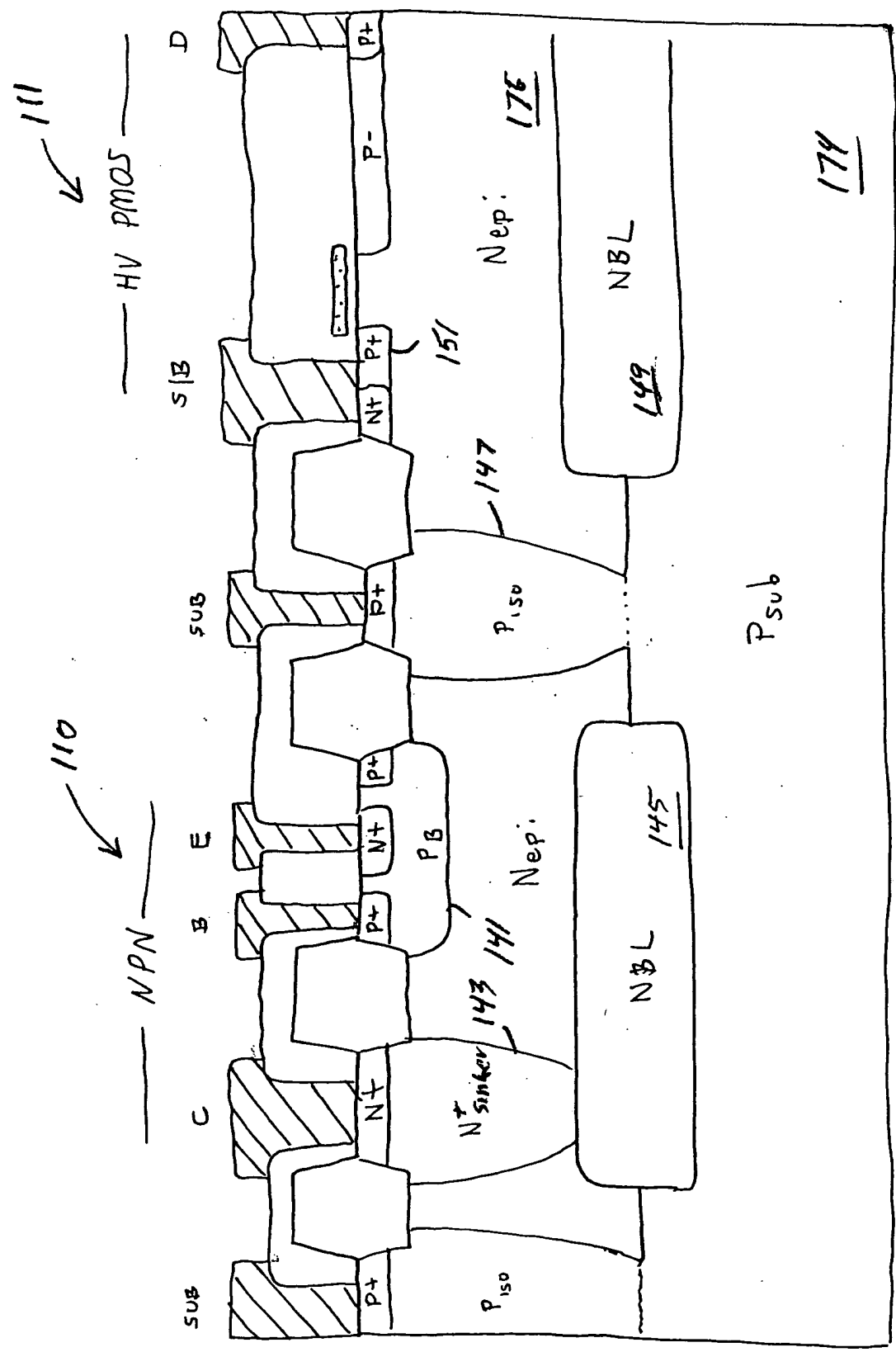
N-ch QVDMOS



9/21/9

Prior Art

Fig. 4C



10/219

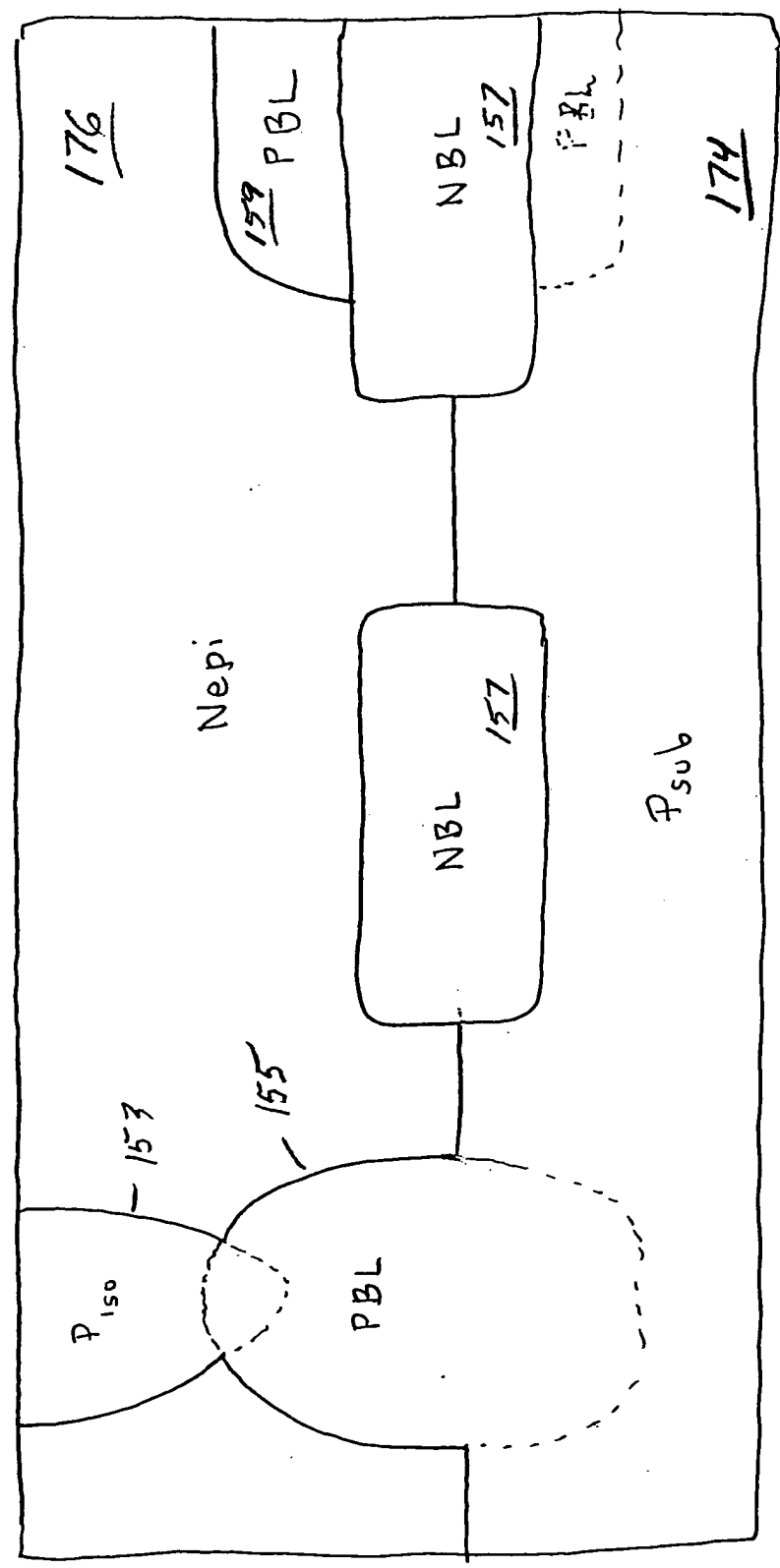
Fig. 5A

Prior Art

P₊ Buried Layer
(isolated)

N₊ Buried Layer

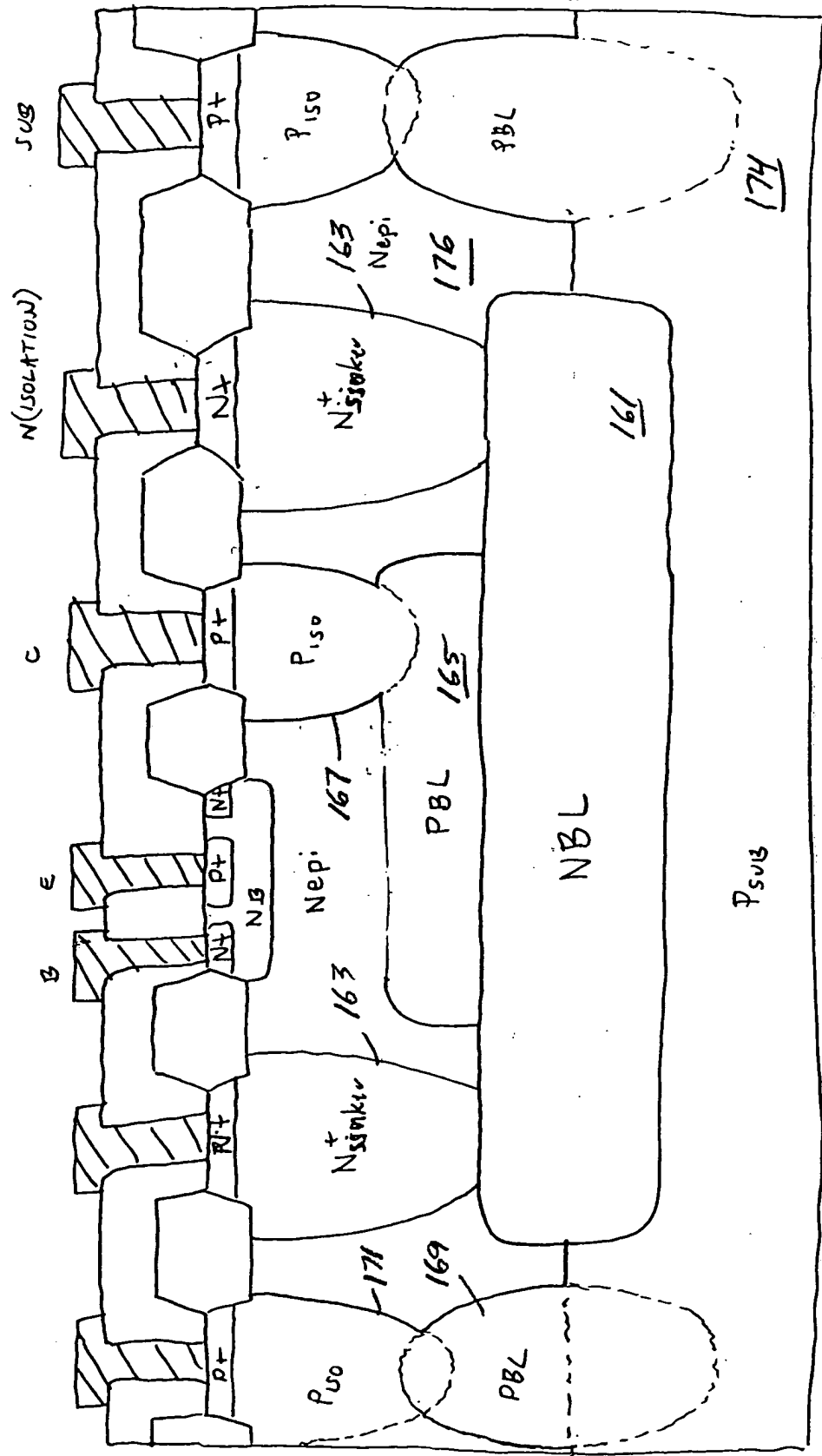
isolation



Fi 5
SB

211

PNP



12/2/19

Fig. 5C

Prior Art

104

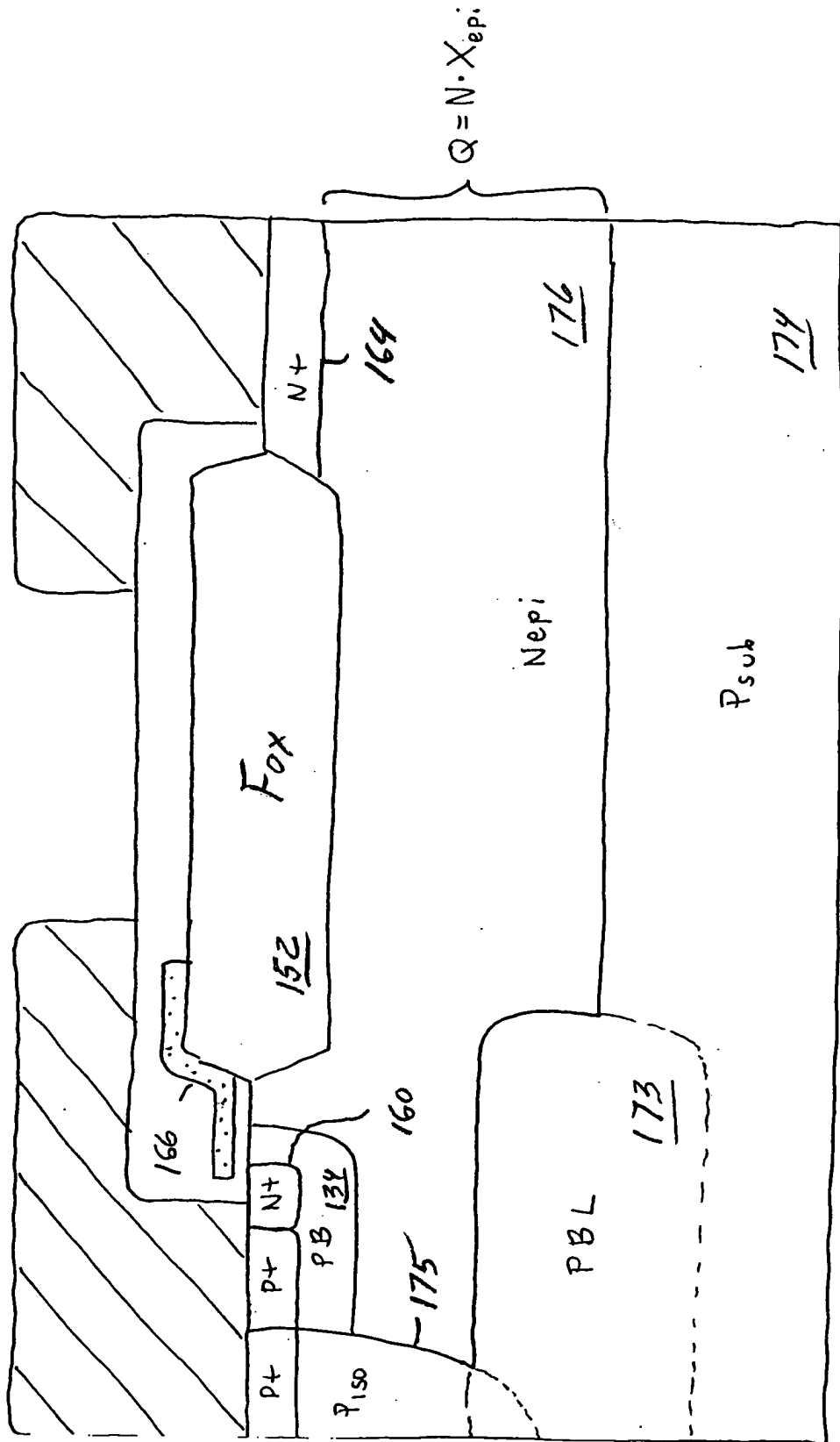
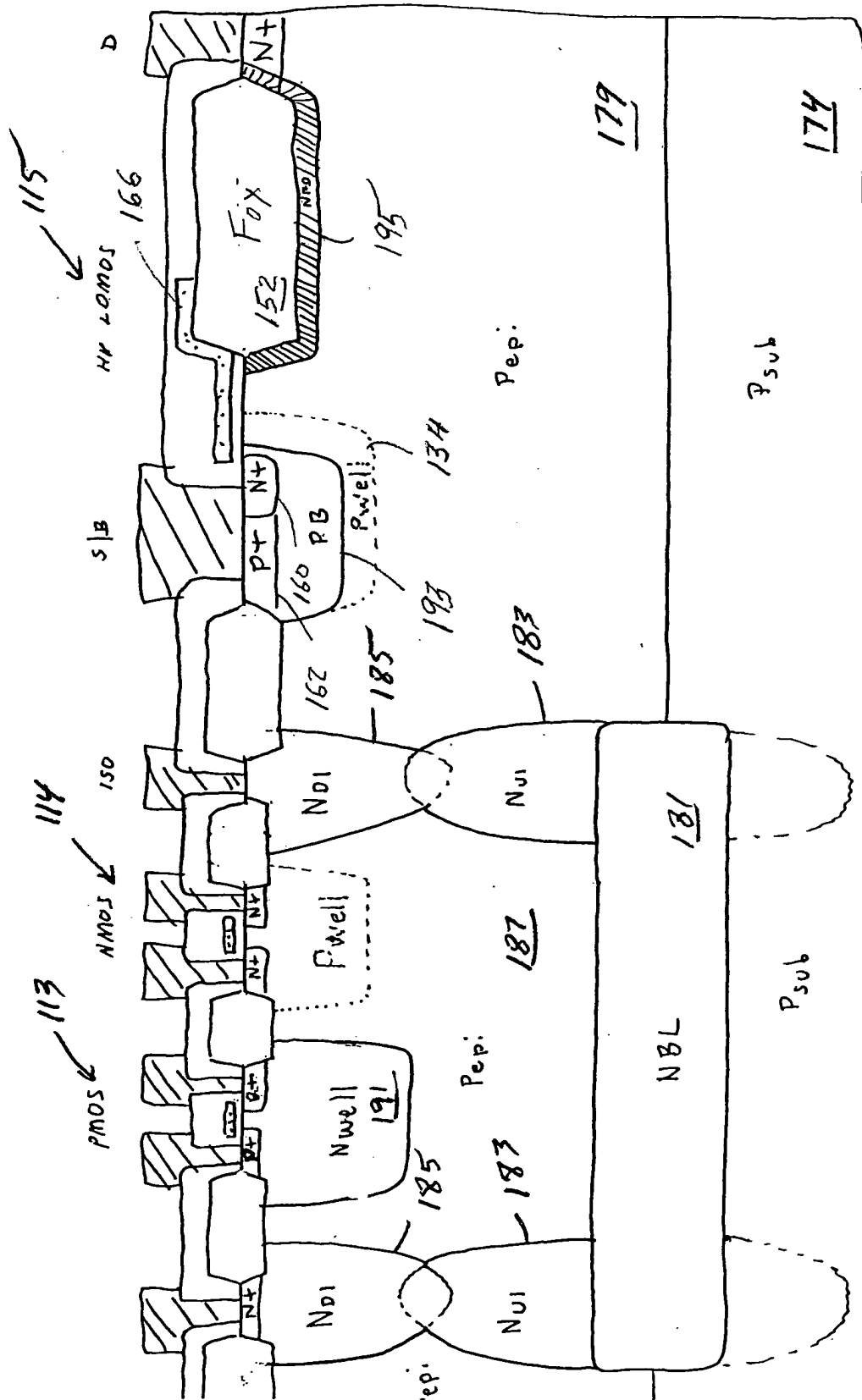


Fig 6A

Prior Art



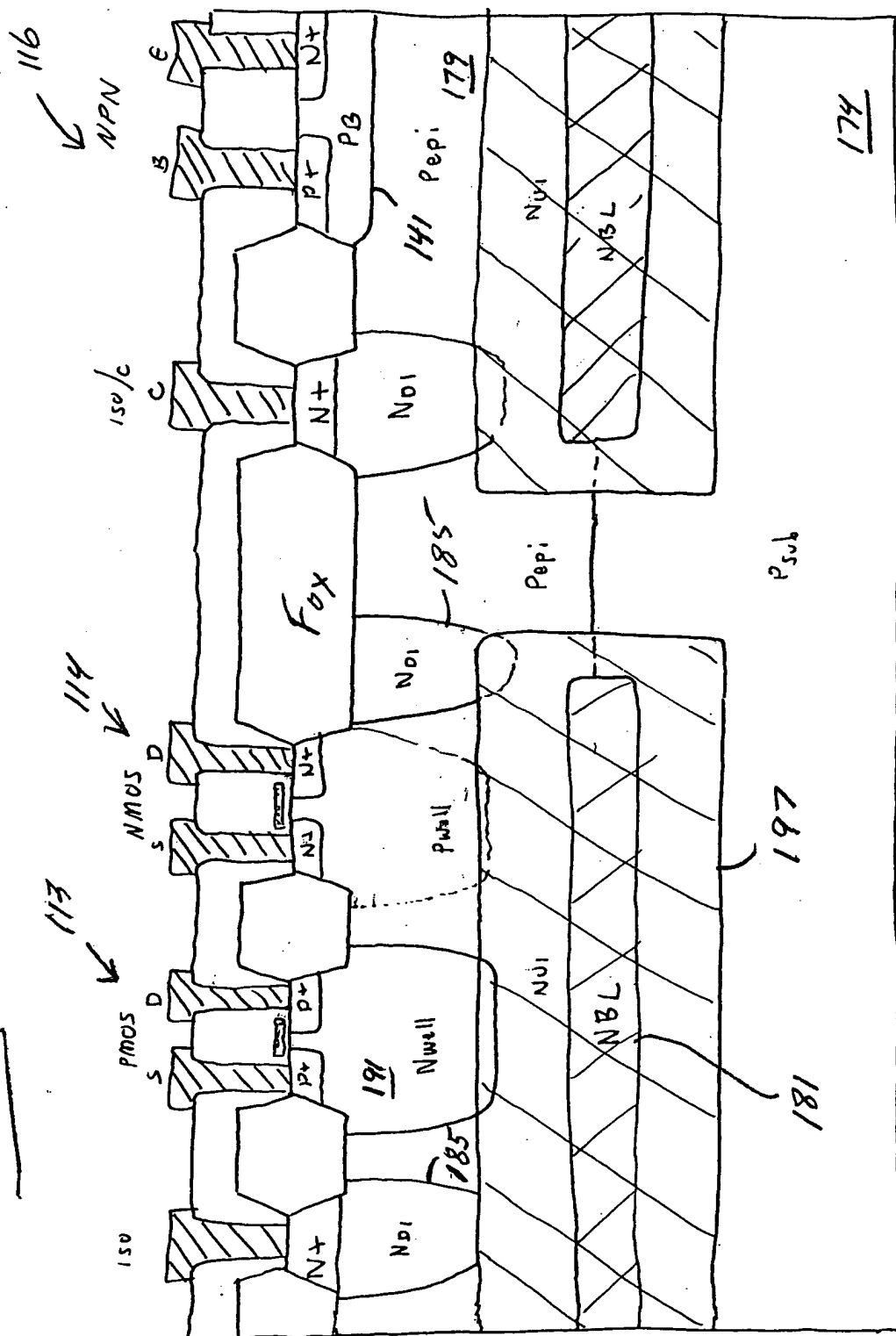
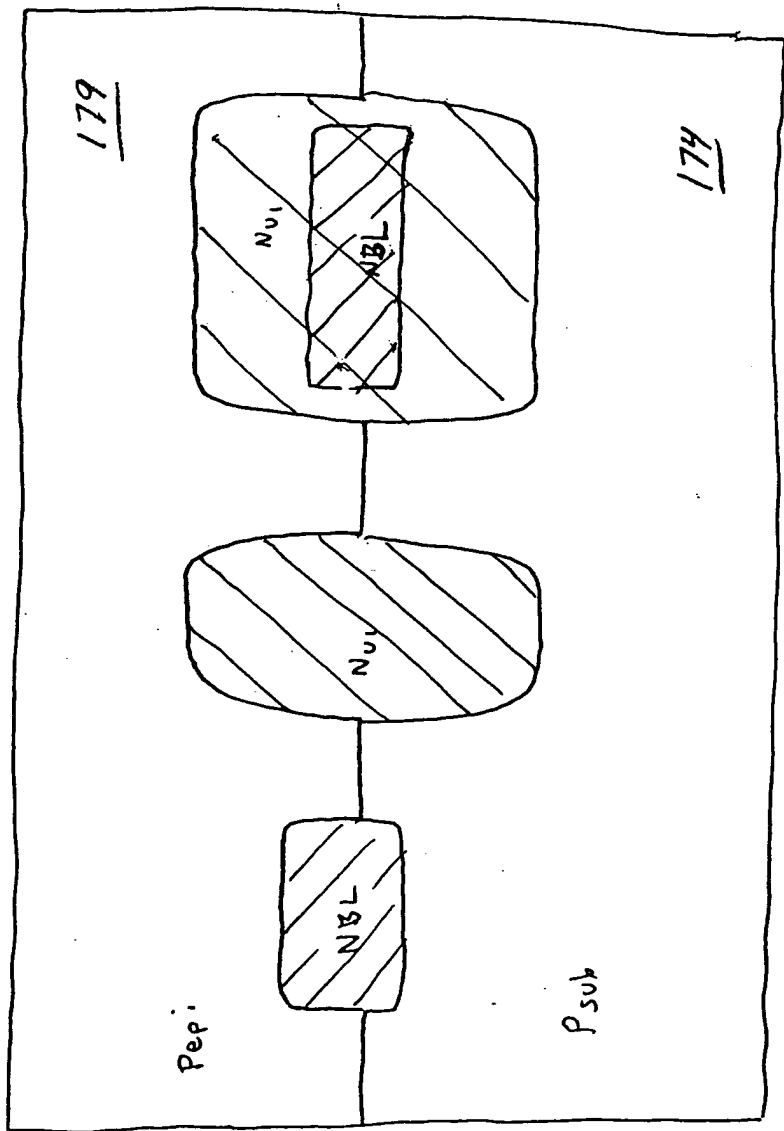


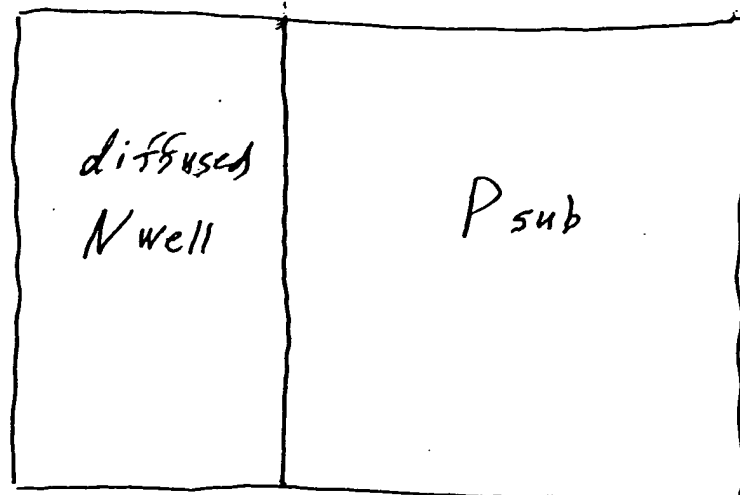
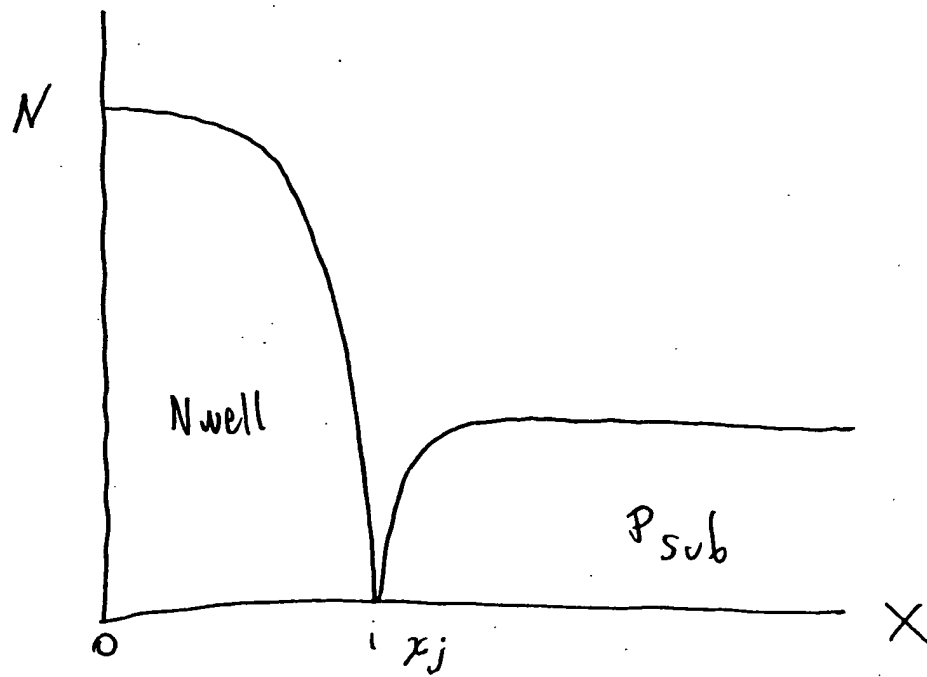
Fig. 6C

Prior Art



17/219

Prior Art Fig. 7A



18/219

Fig. 7B

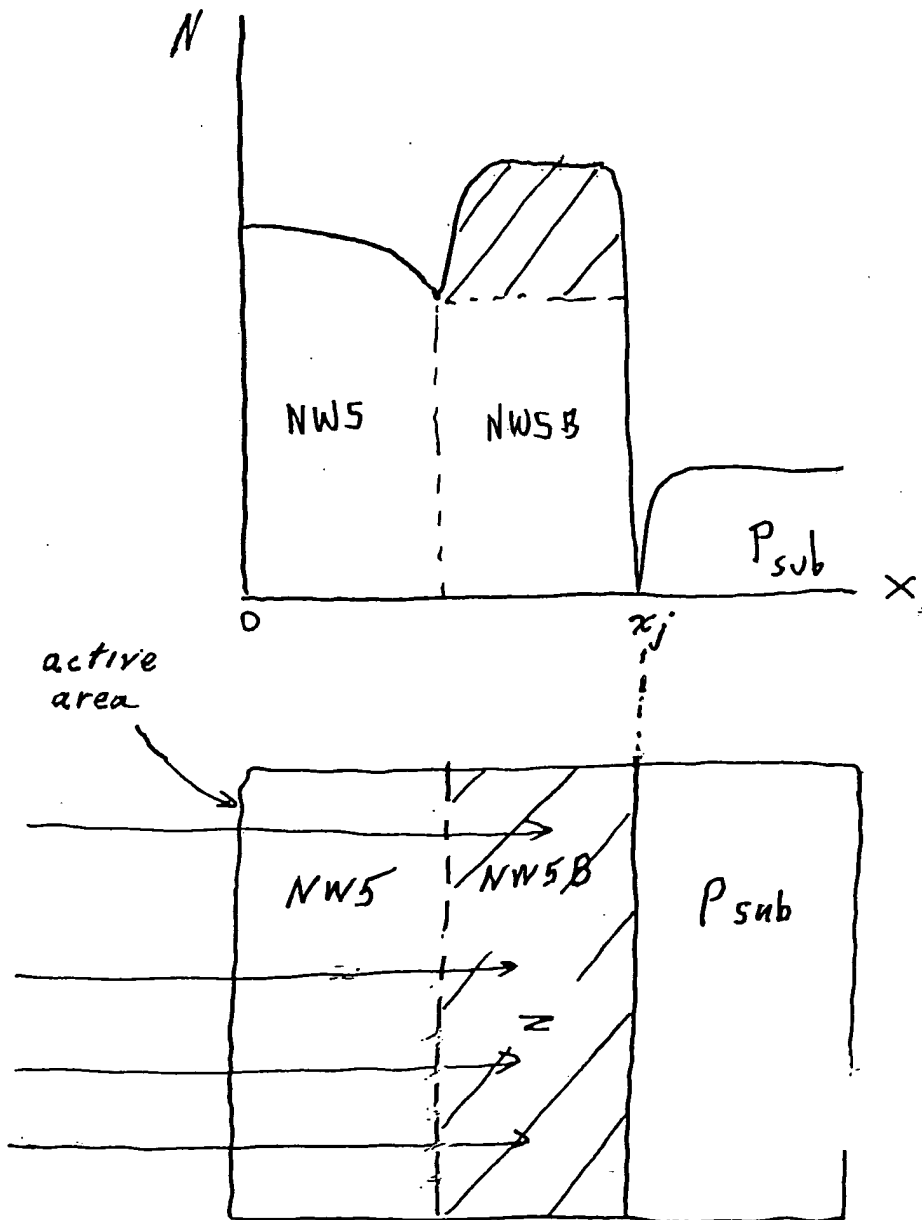
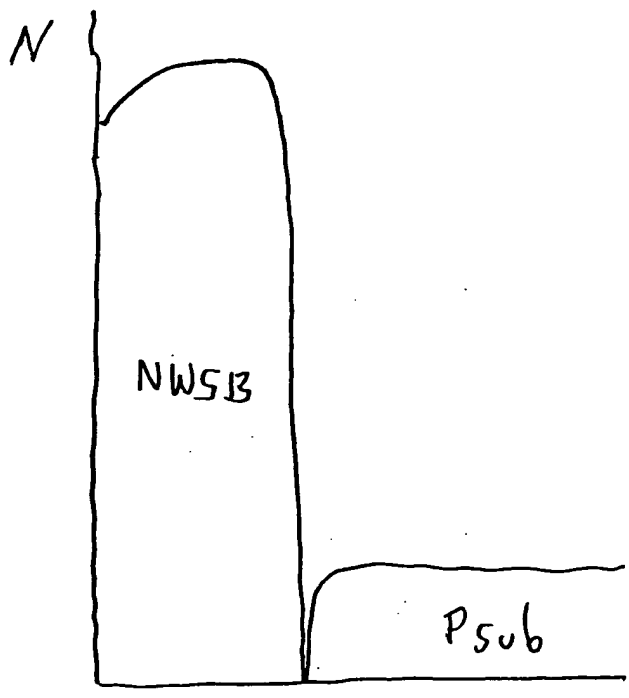
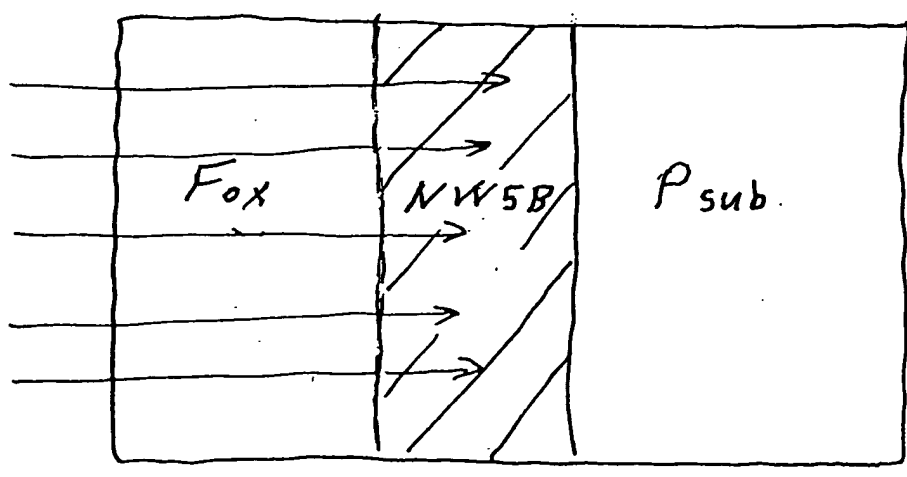
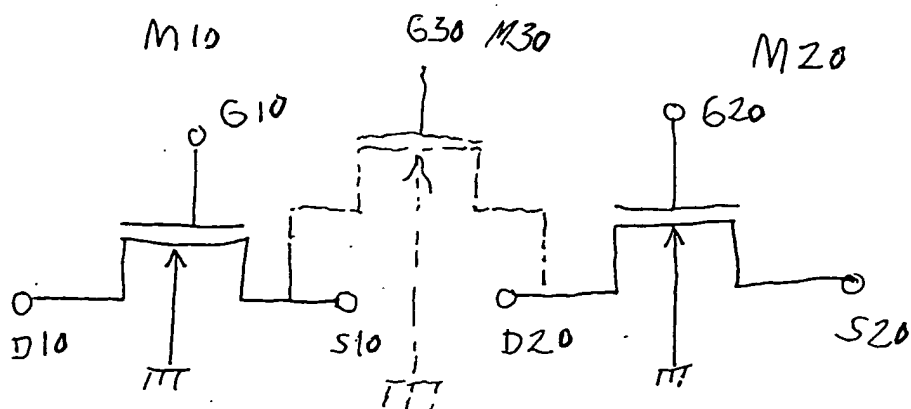


Fig. 7c



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21/219

Fig. 9B

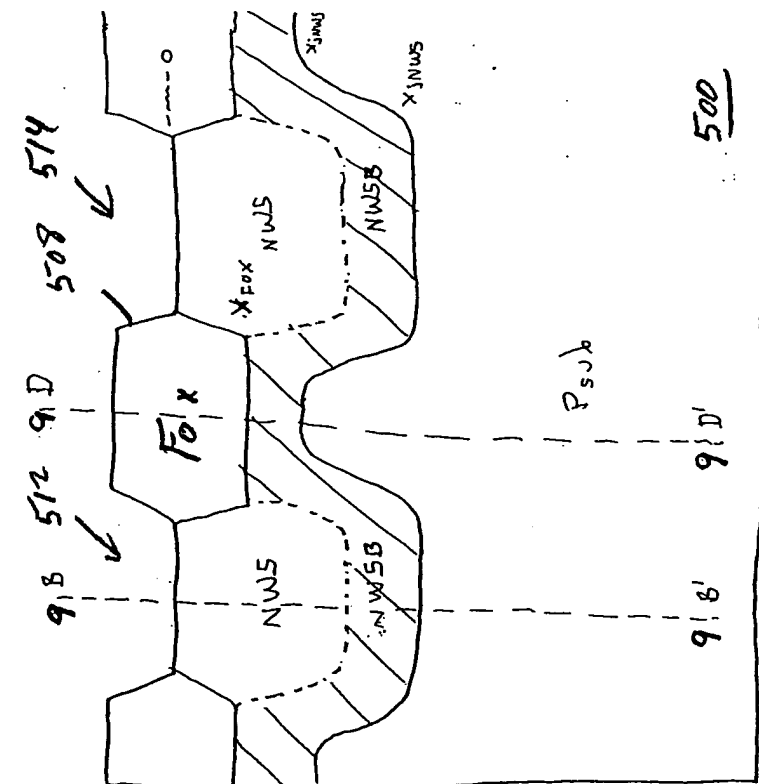
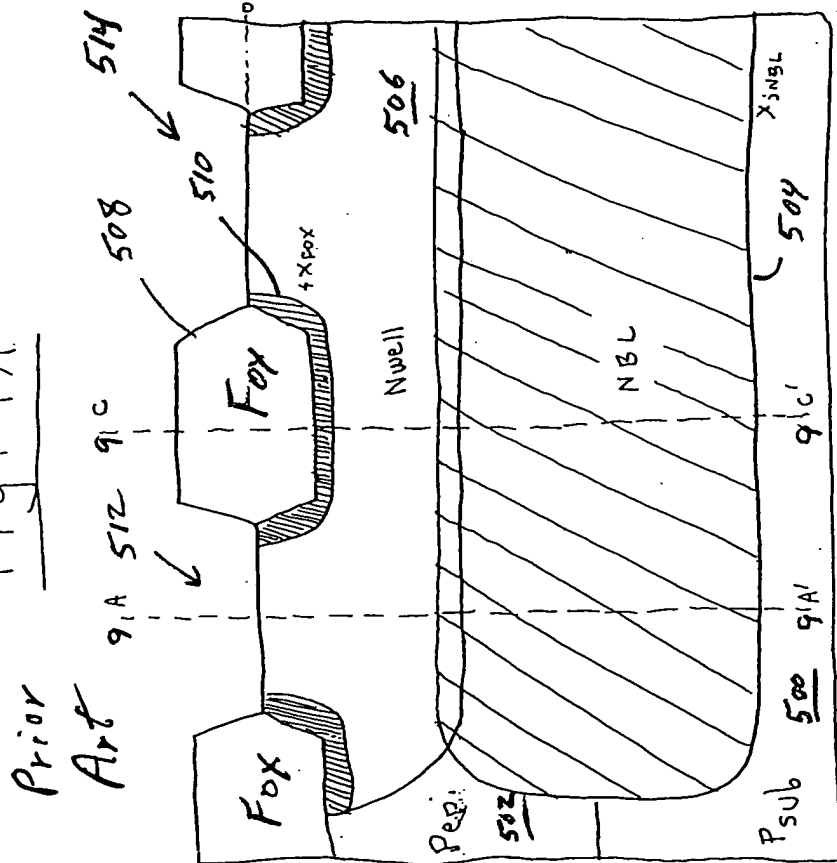


Fig. 9A



Prior

Art

Prior
Art

Fig. 9C

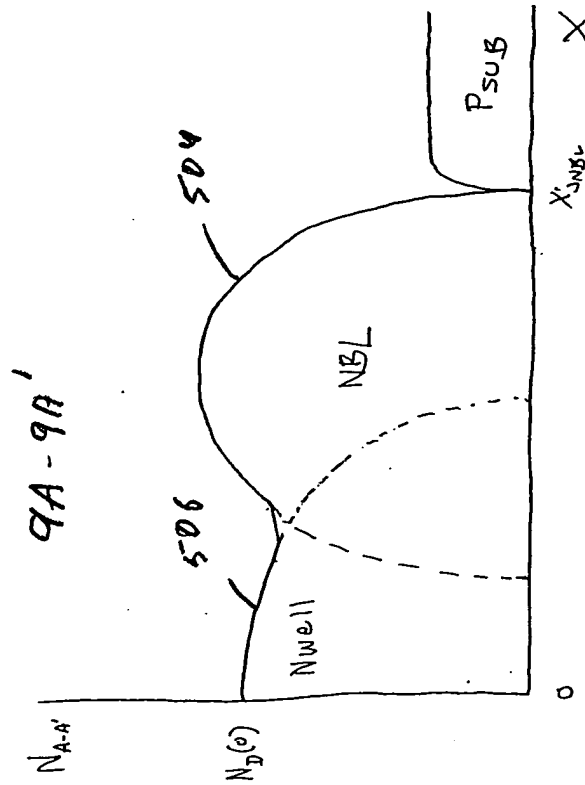
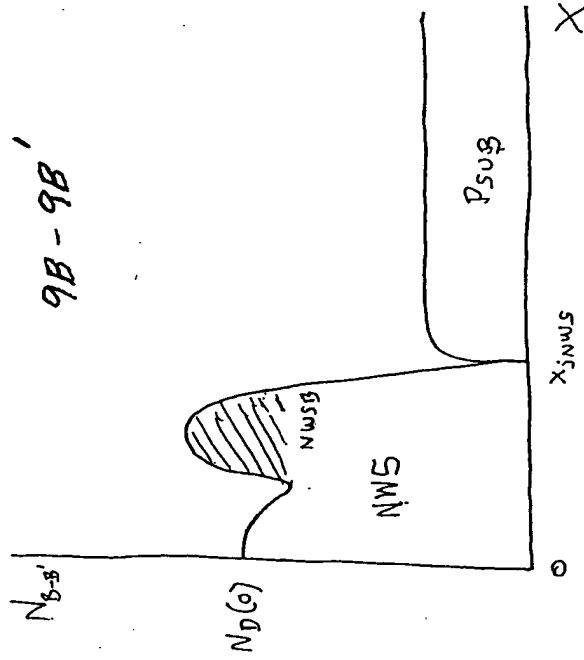


Fig. 9D



Prior Art

Fig. 9E

9C-9C'

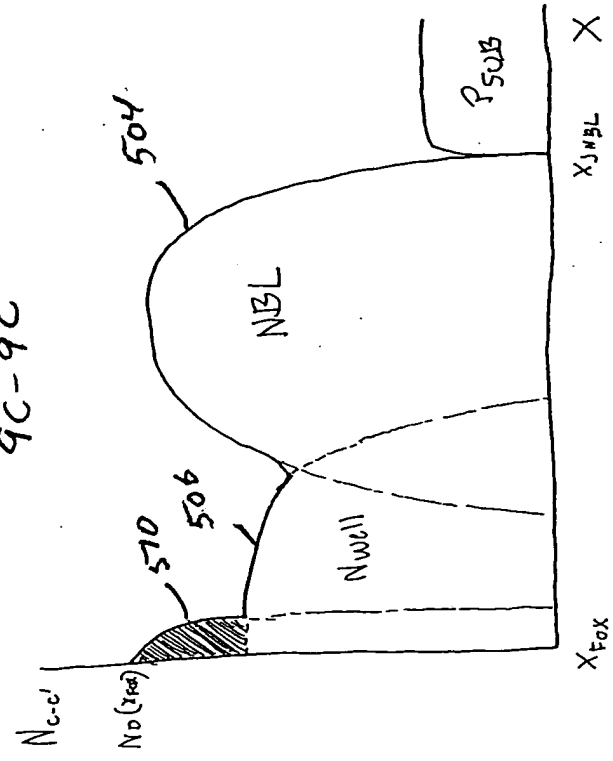


Fig. 9F

9D-9D'

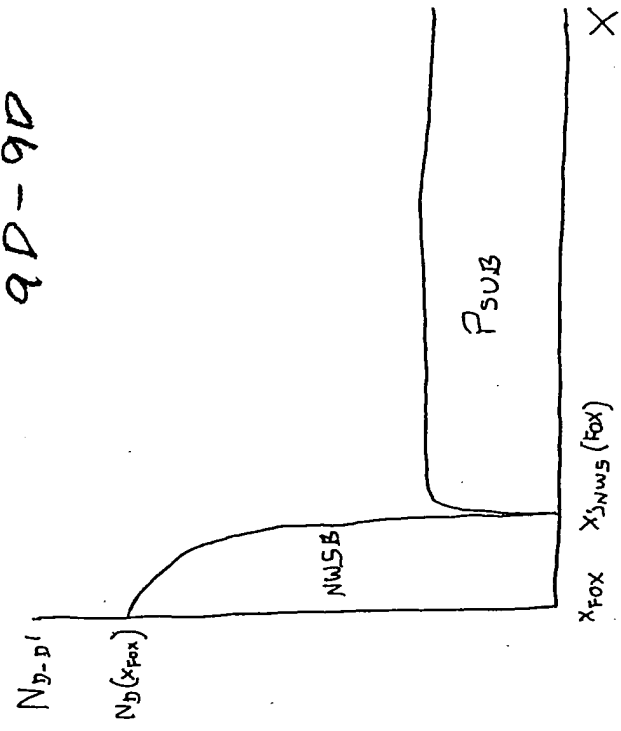


Fig. 10B

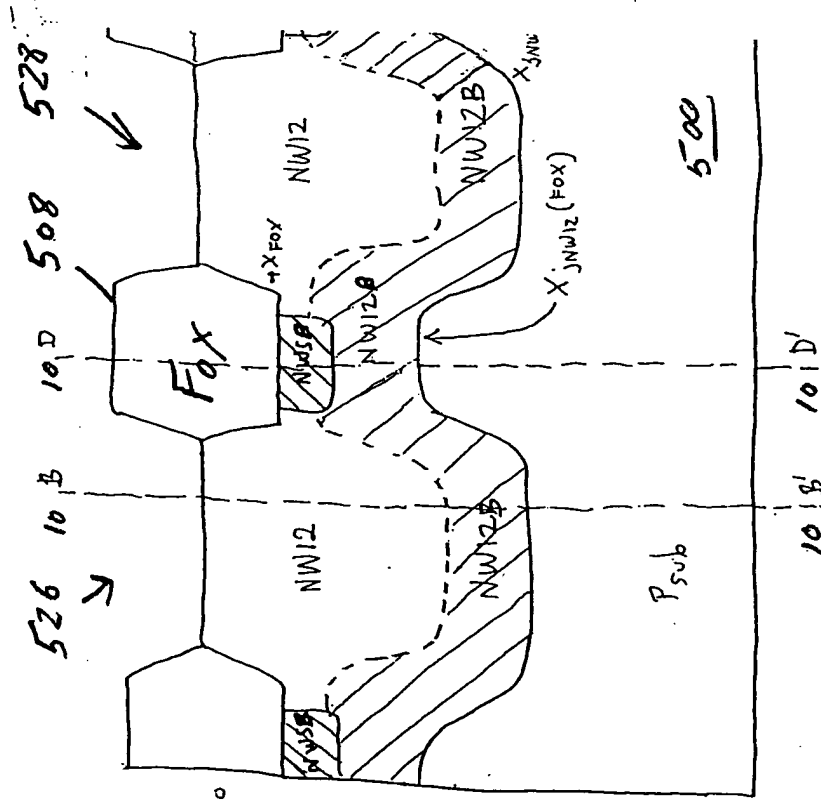
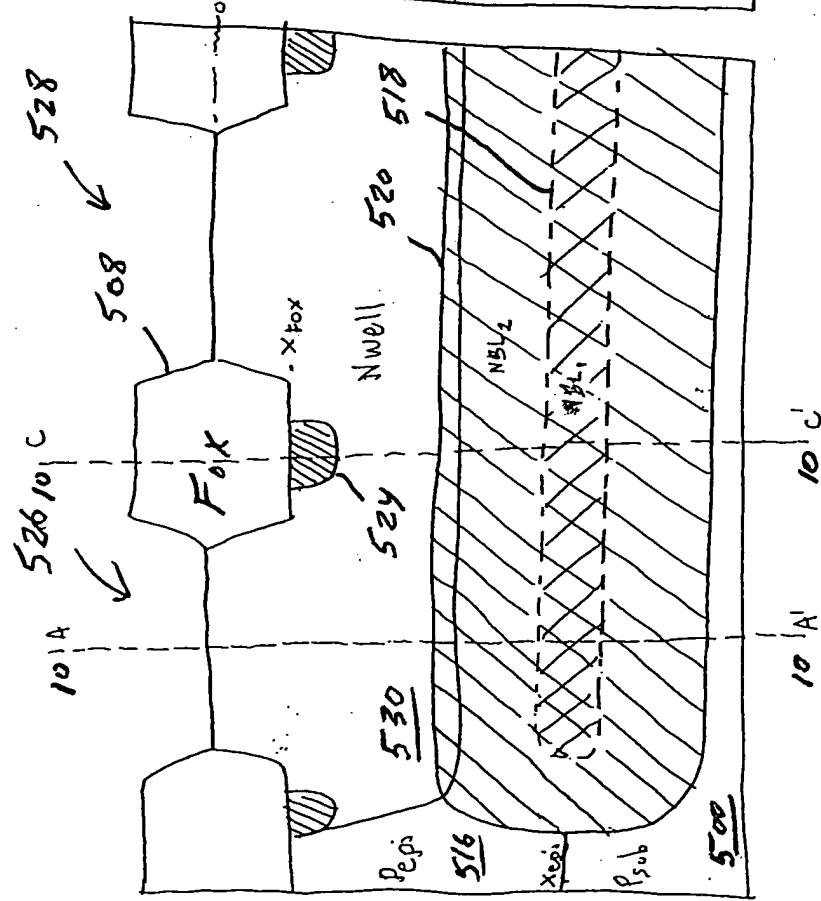


Fig. 10D

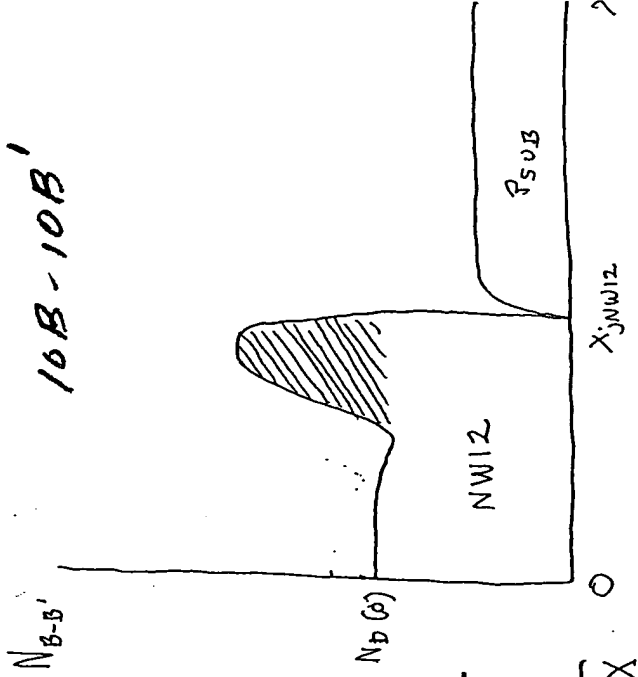


Fig. 10C

Prior

Art 10A-10A'

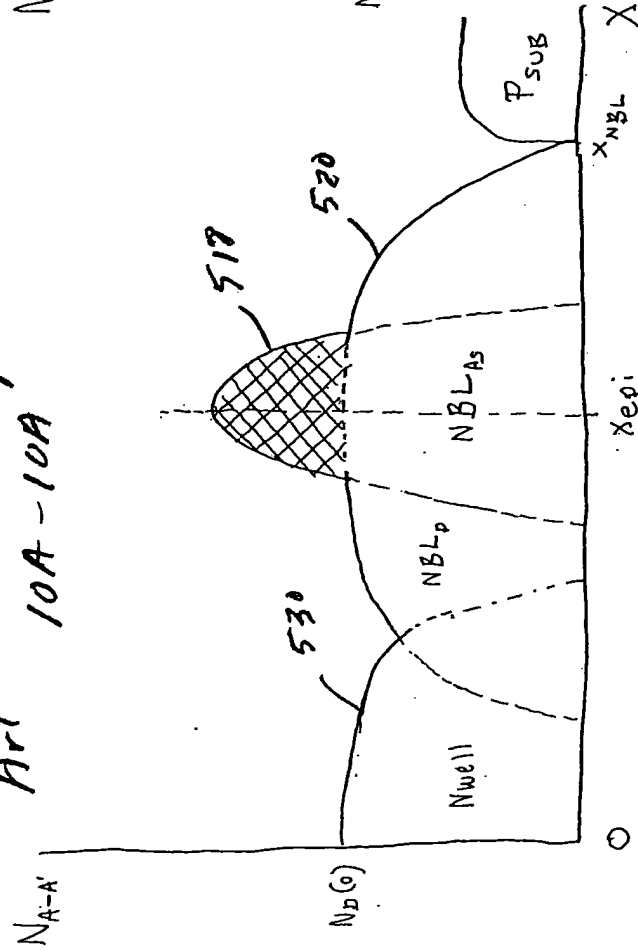


Fig. 10F

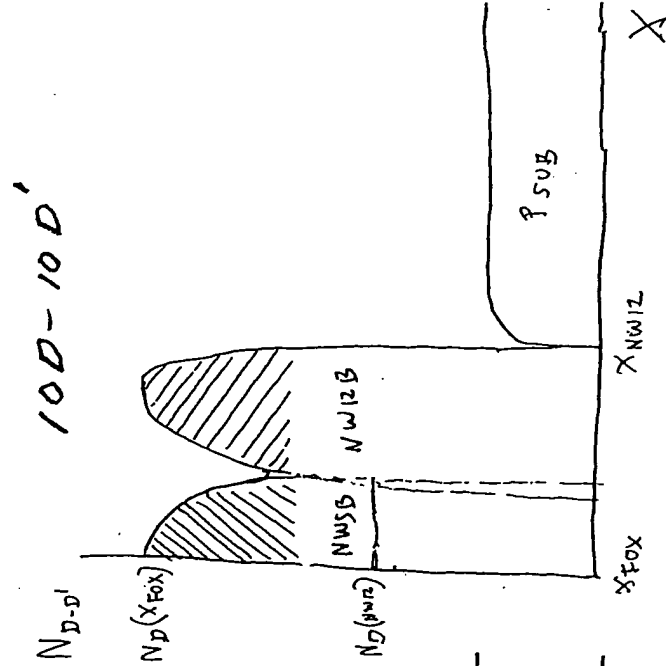


Fig. 10E

Prior Art

10C-10C'

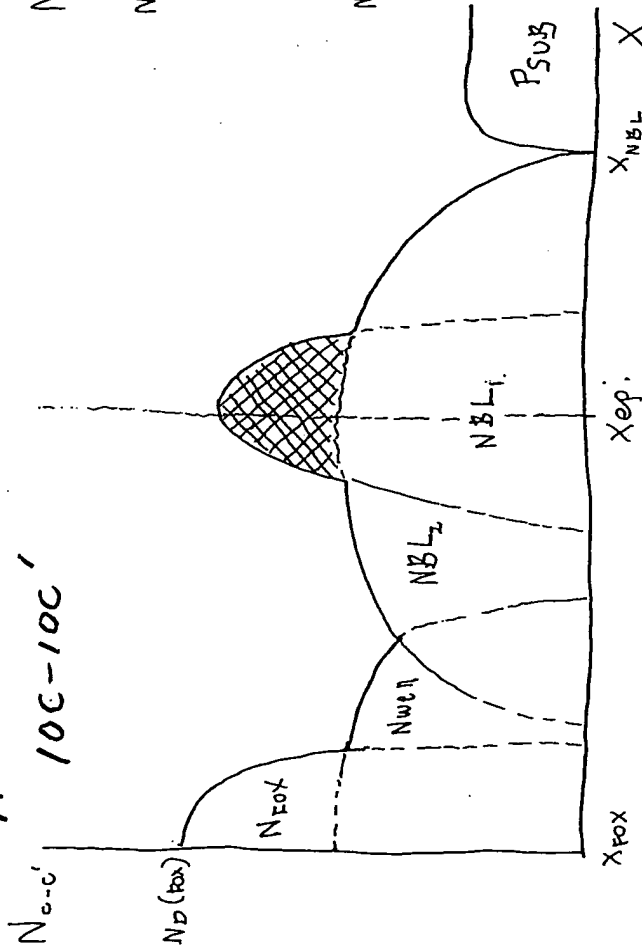


Fig. 10G

10D-10D'

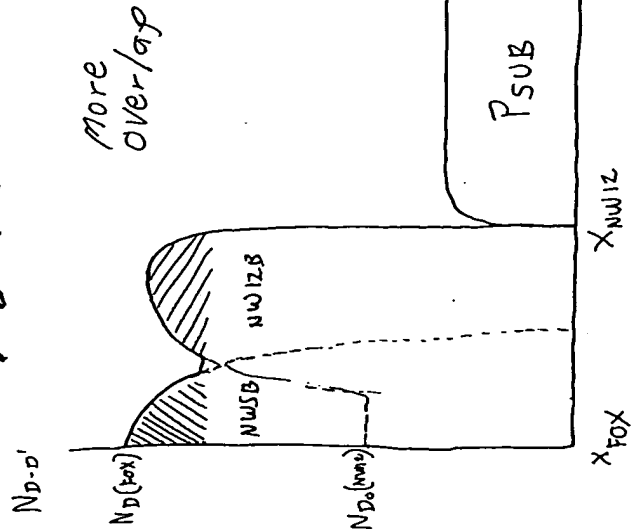


Fig. 10H

10D-10D'

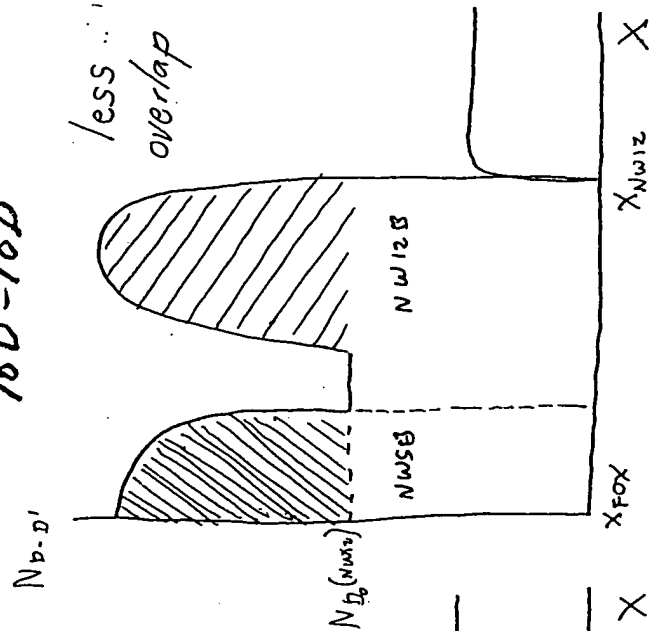
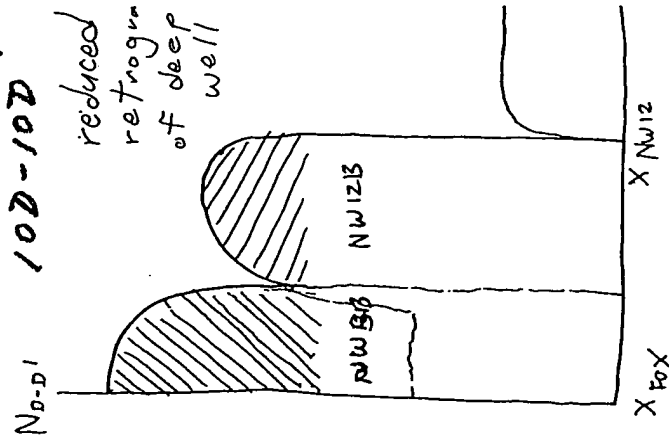
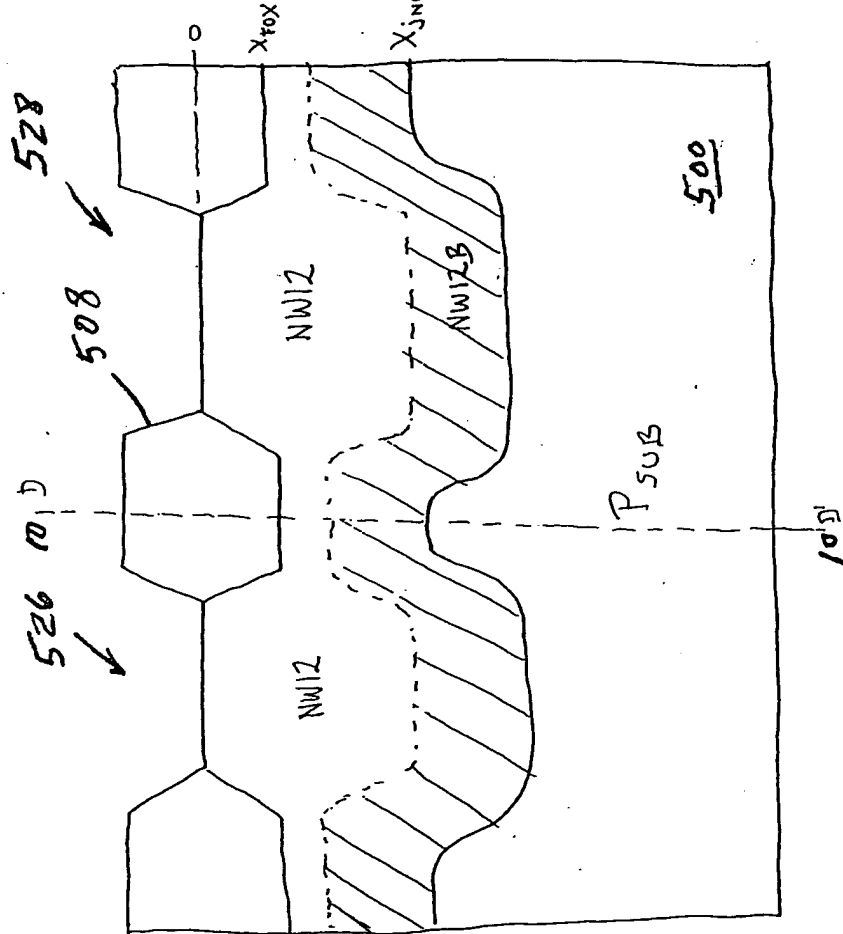


Fig. 10I

10D-10D'



70
5
4



102

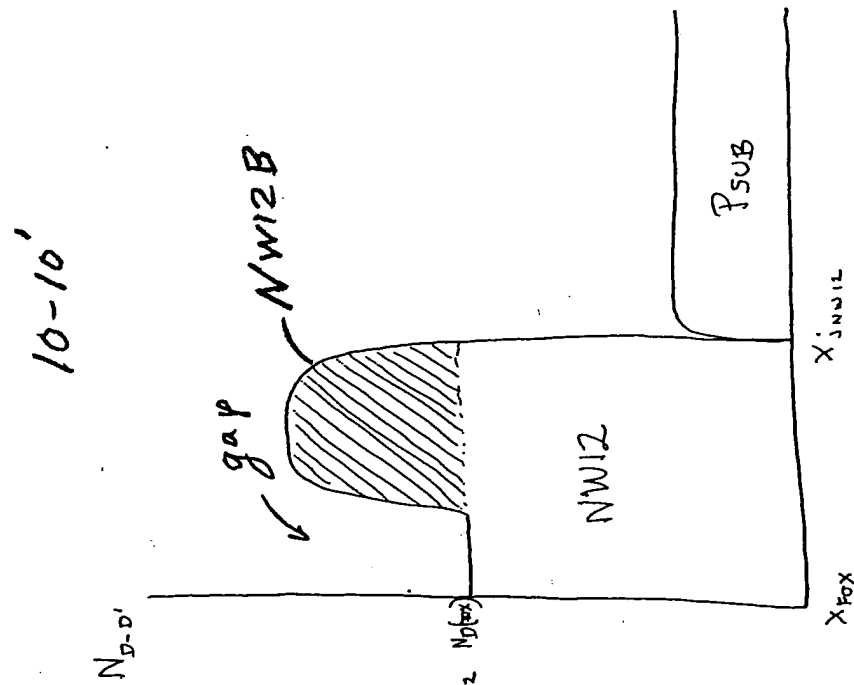
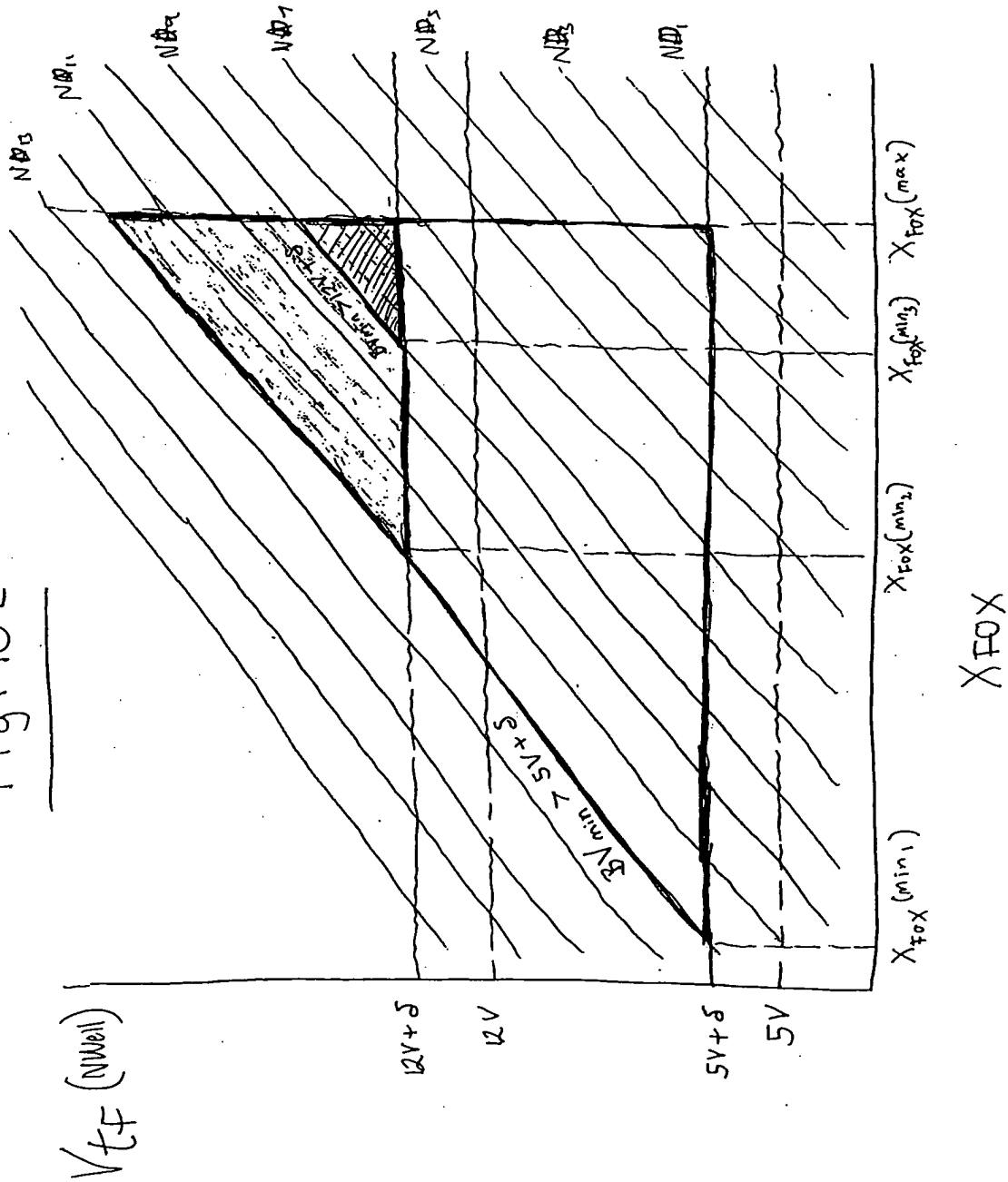


Fig. 10L



Fi 5.11A

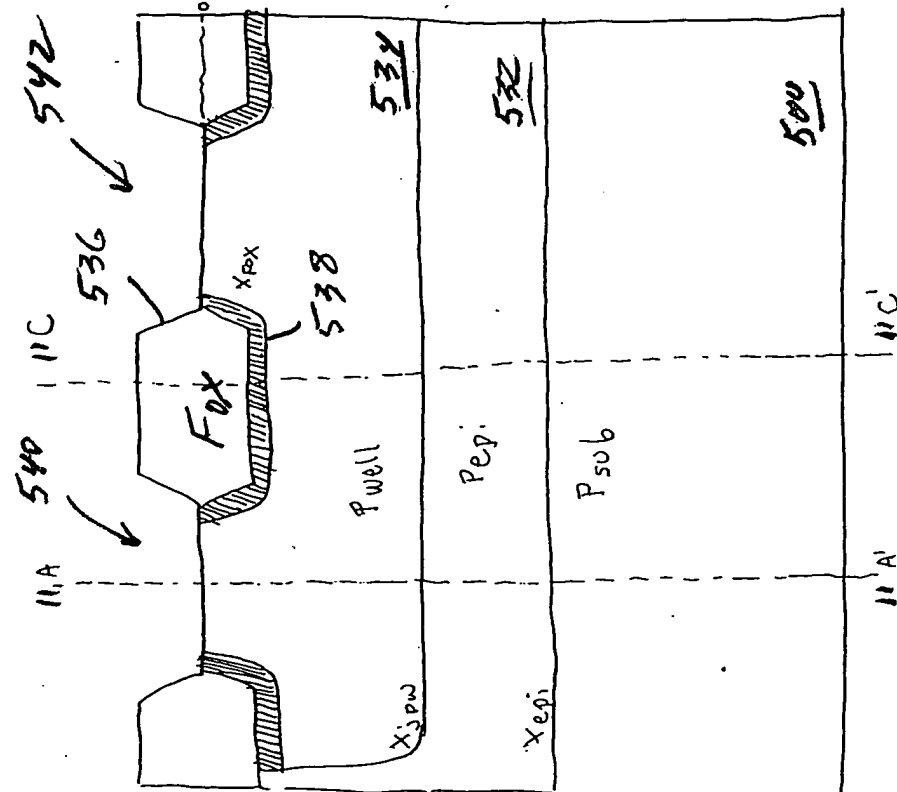


Fig. 11B

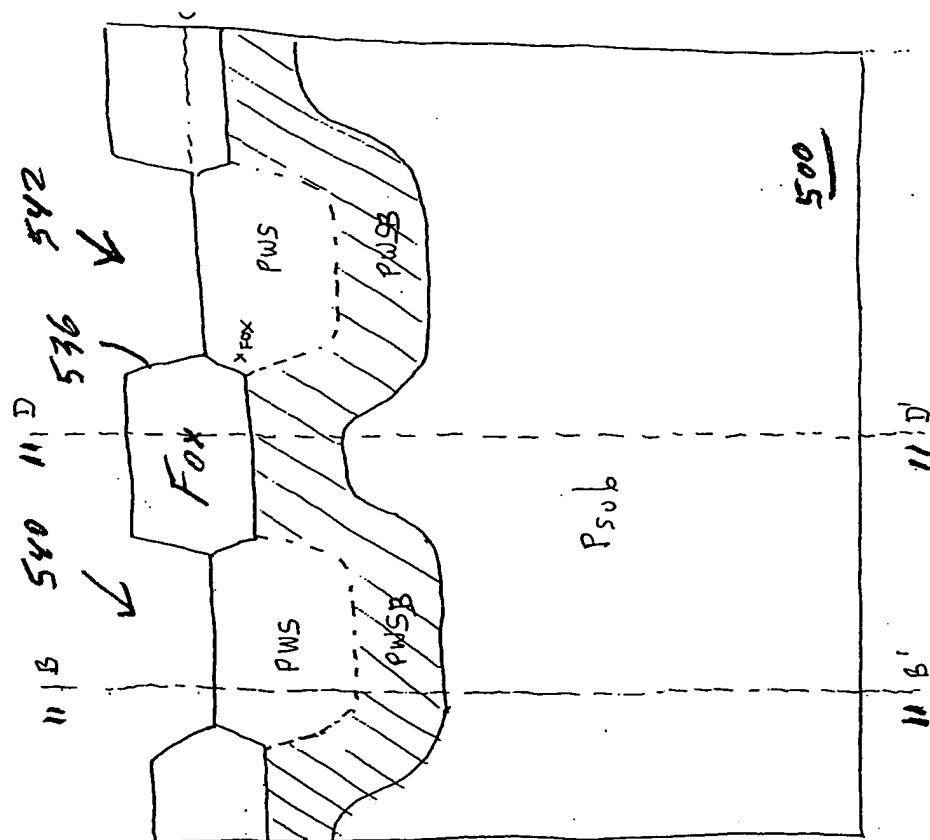


Fig. 11C

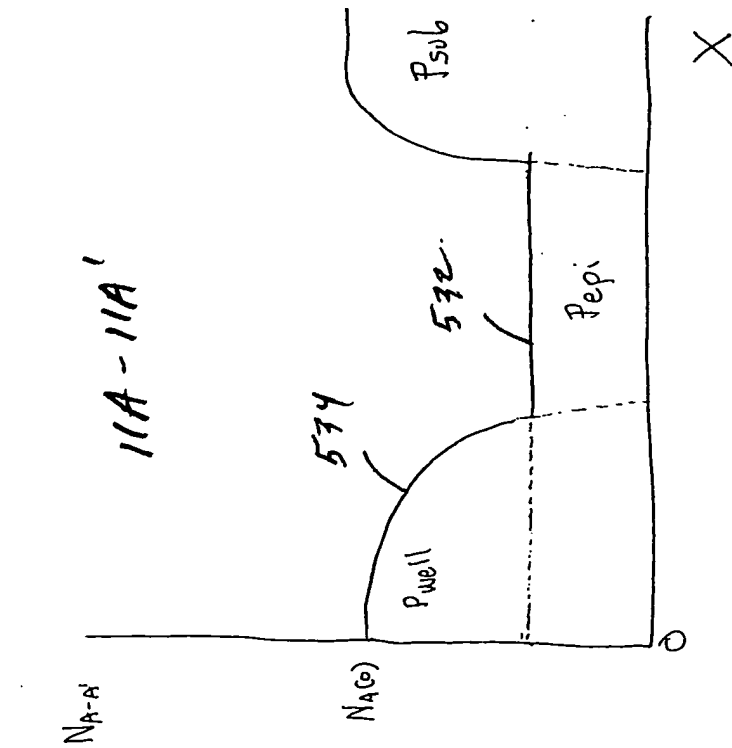


Fig. 11D

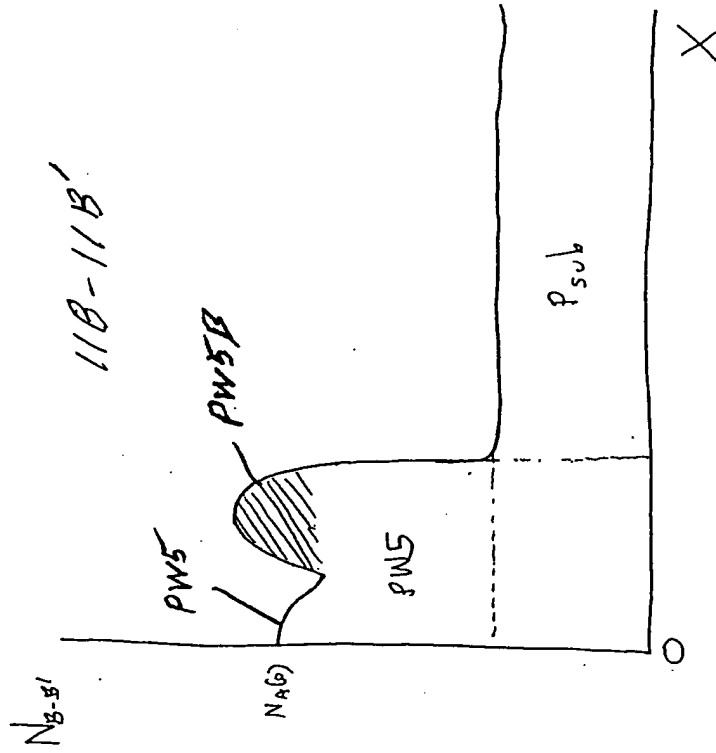


Fig. 11E

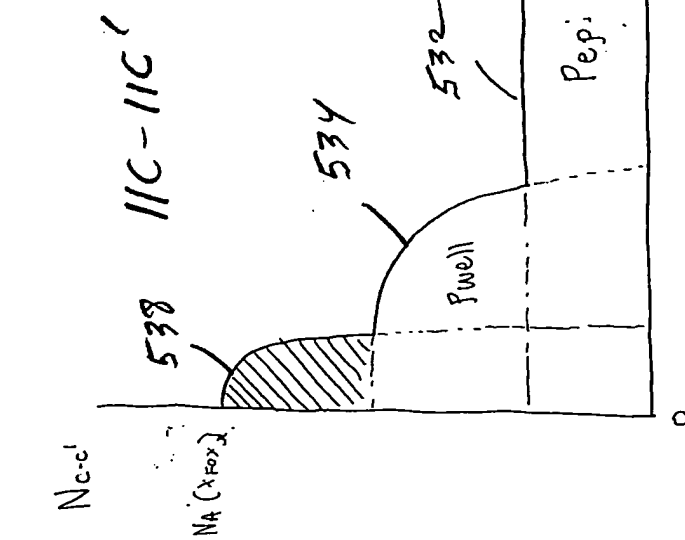


Fig. 11F

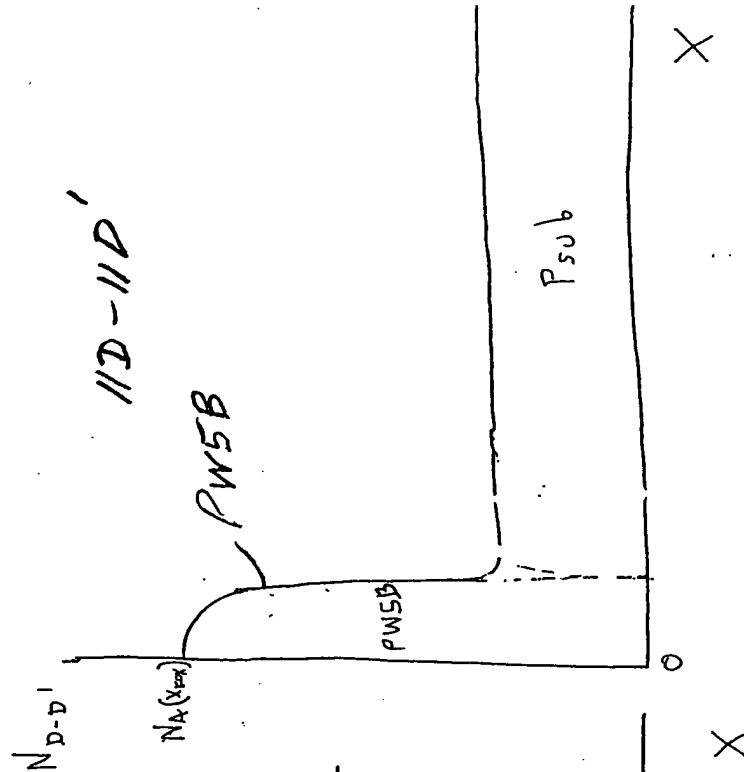


Fig. 11H

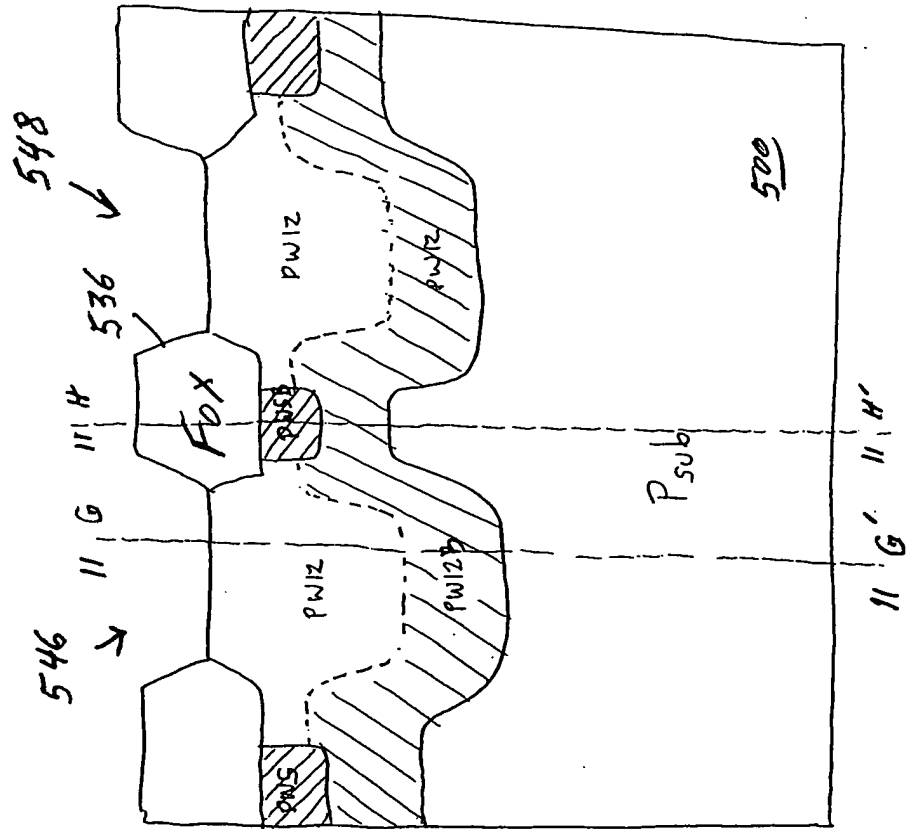


Fig. 11G

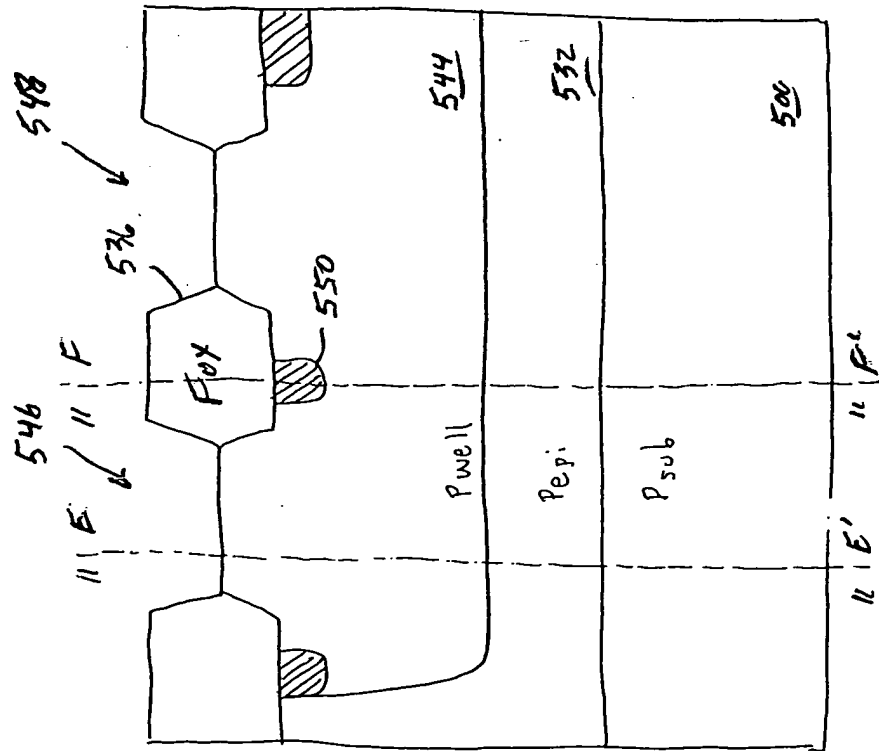


Fig. 11I

11E-11E'

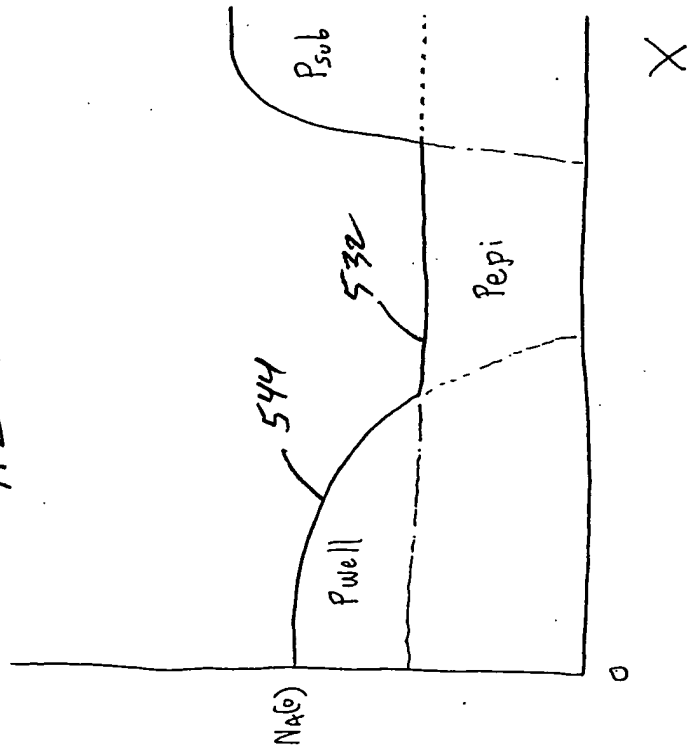


Fig. 11J

11G-11G'

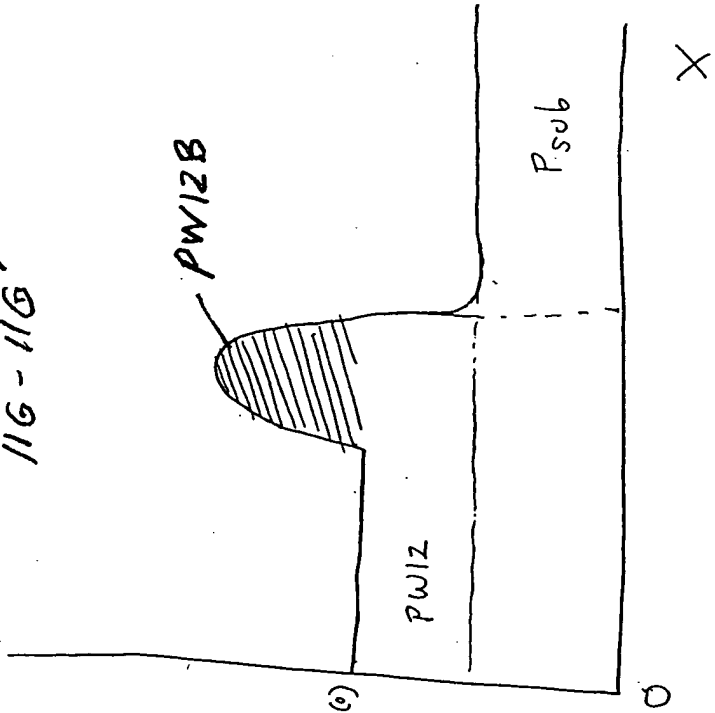


Fig. 11K

11F-11F'

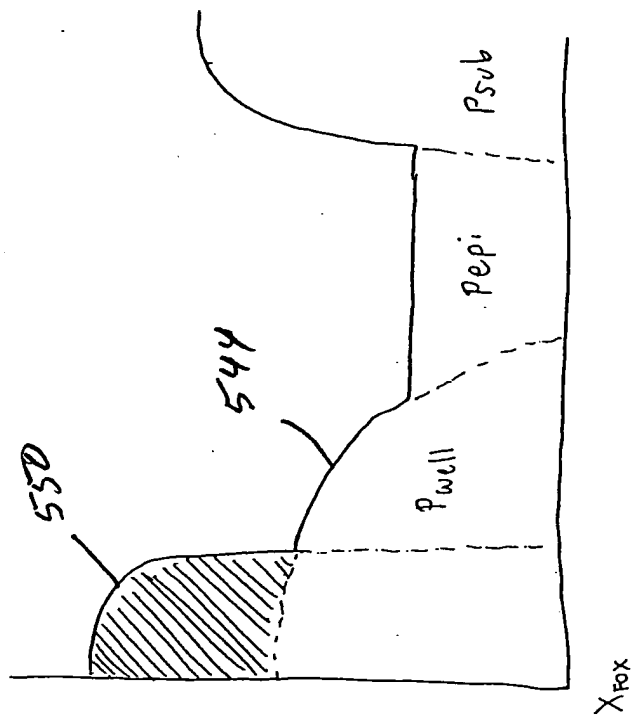


Fig. 11L

11H-11H'

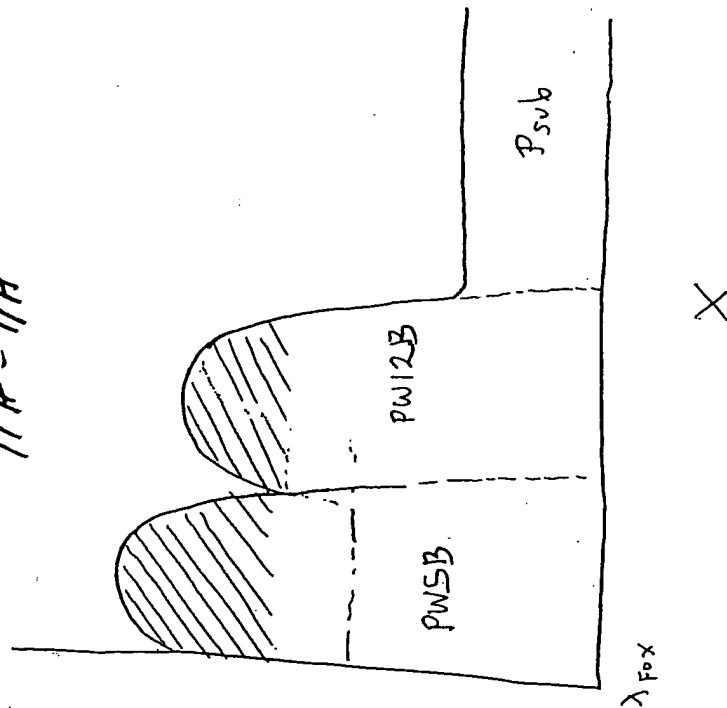


Fig. 12A
epitaxial

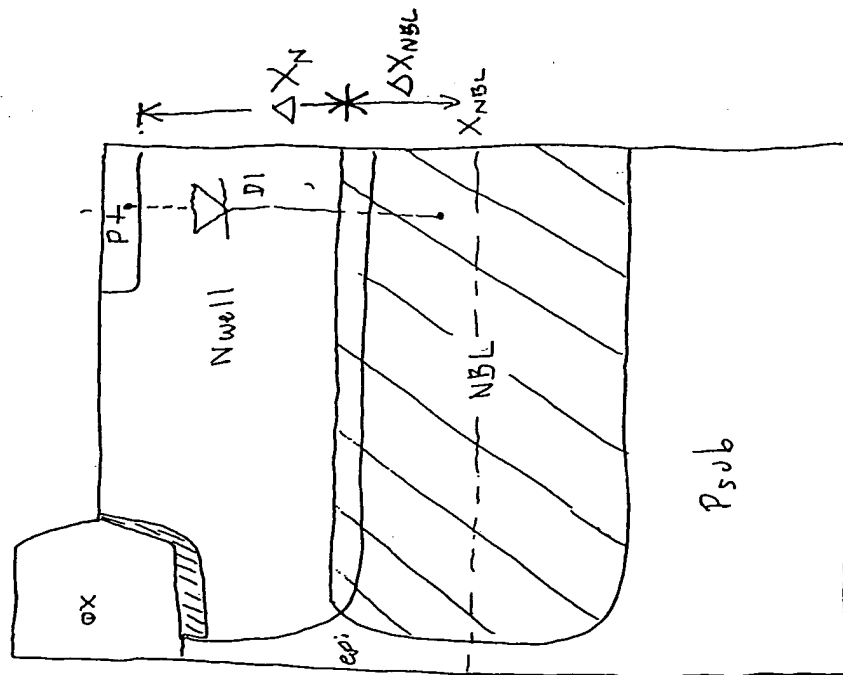


Fig. 12B

implanted

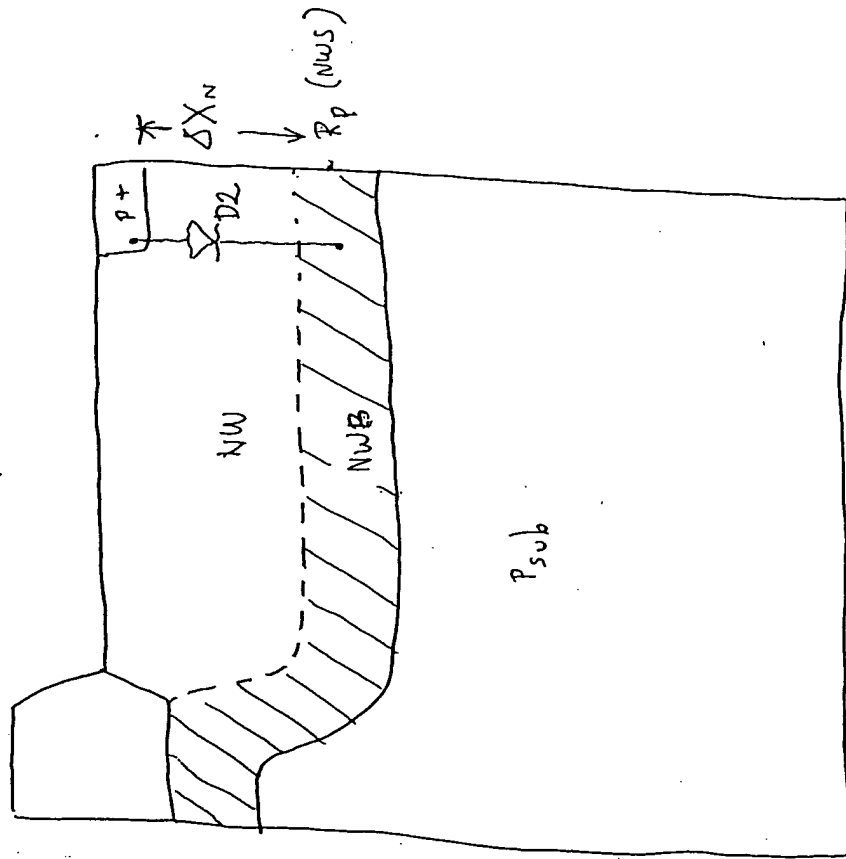


Fig. 12C

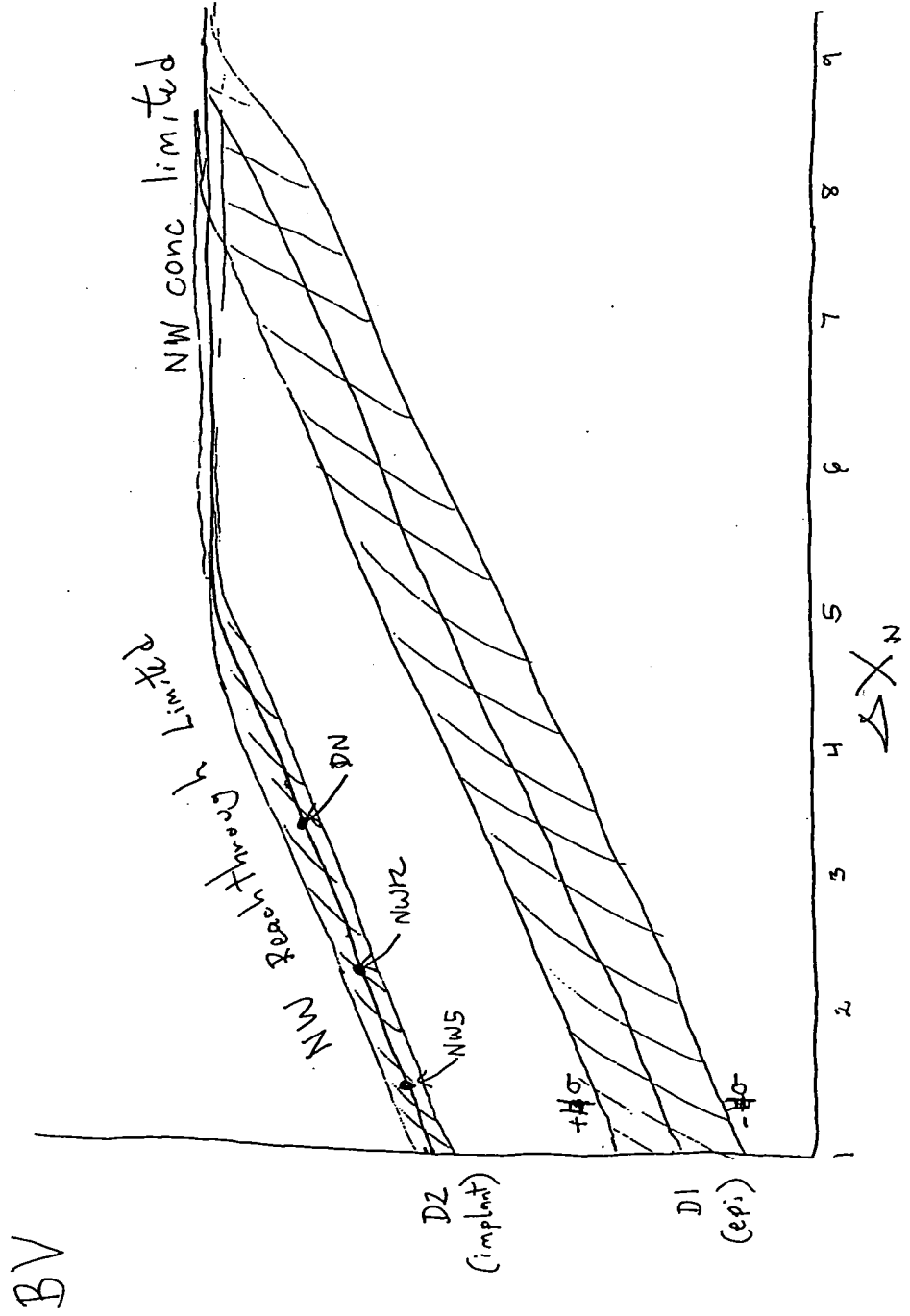


Fig. 13A

Prior
Art

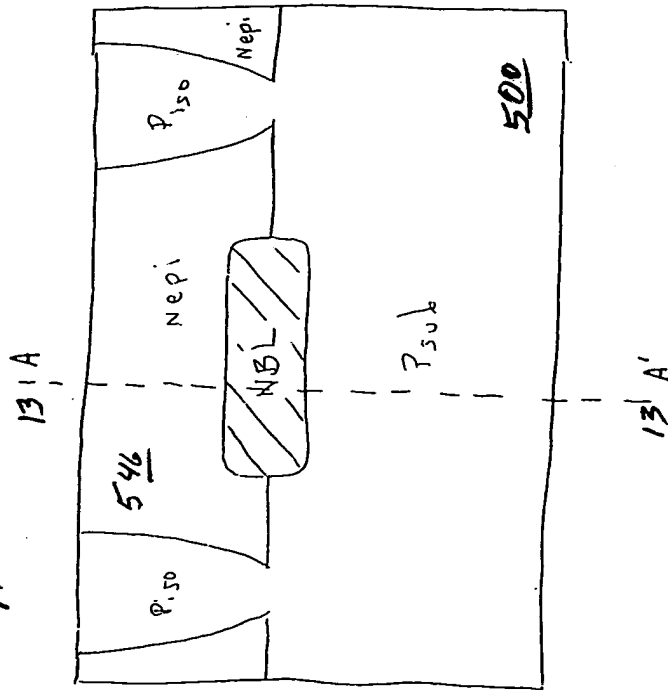


Fig. 13B

Prior
Art

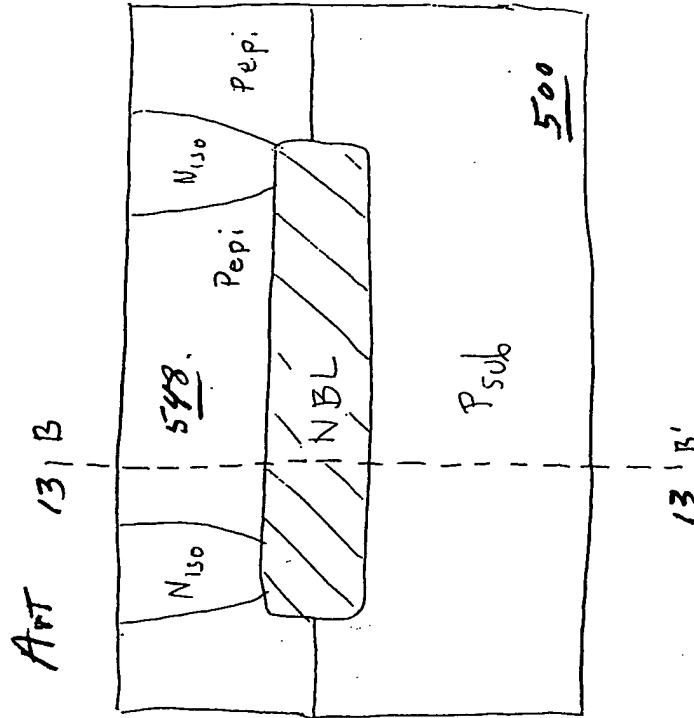


Fig 13C

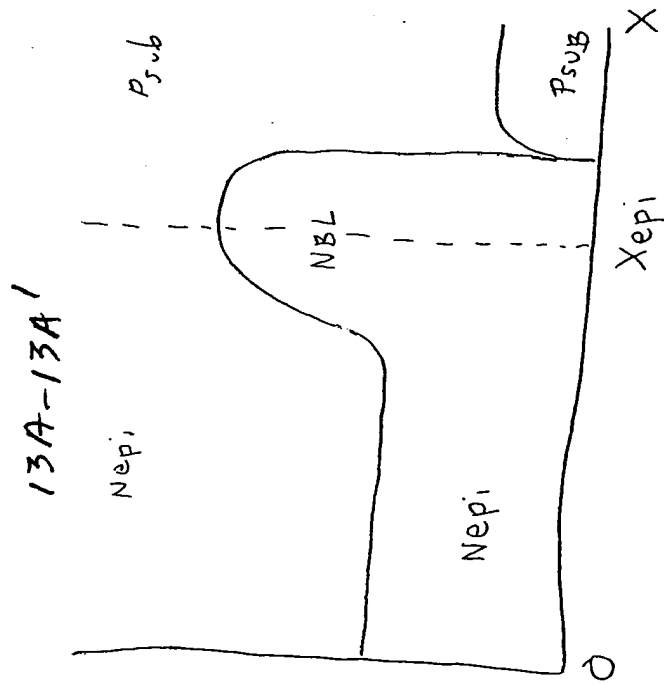


Fig 13D

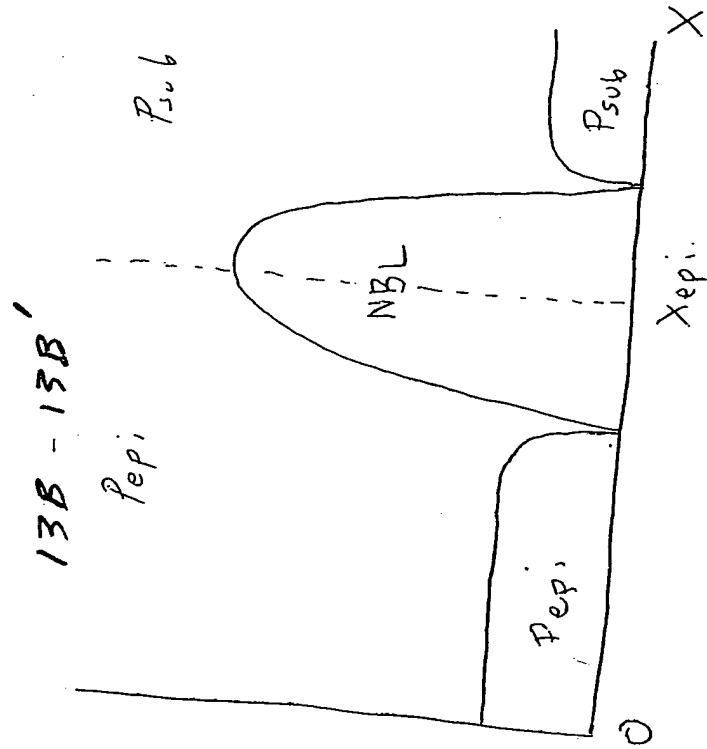


Fig. 13G

13C-13C'

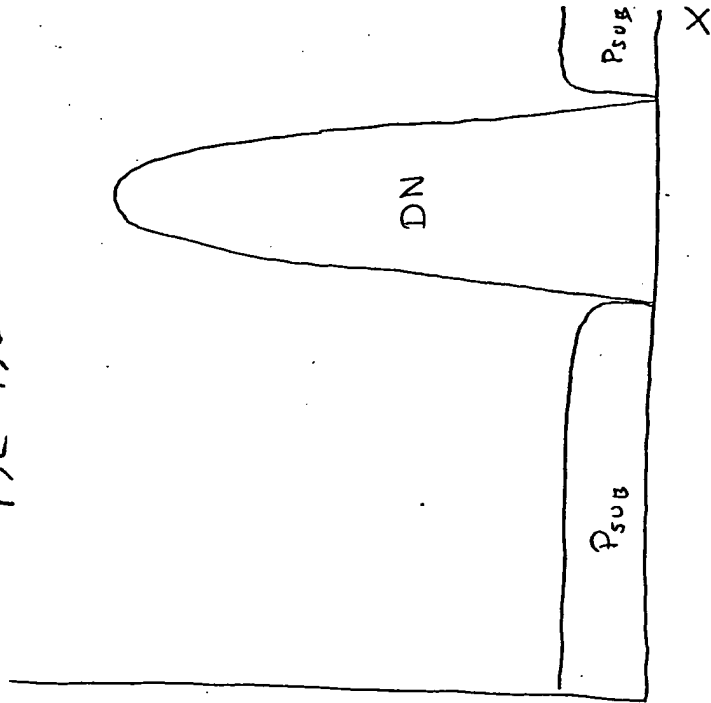
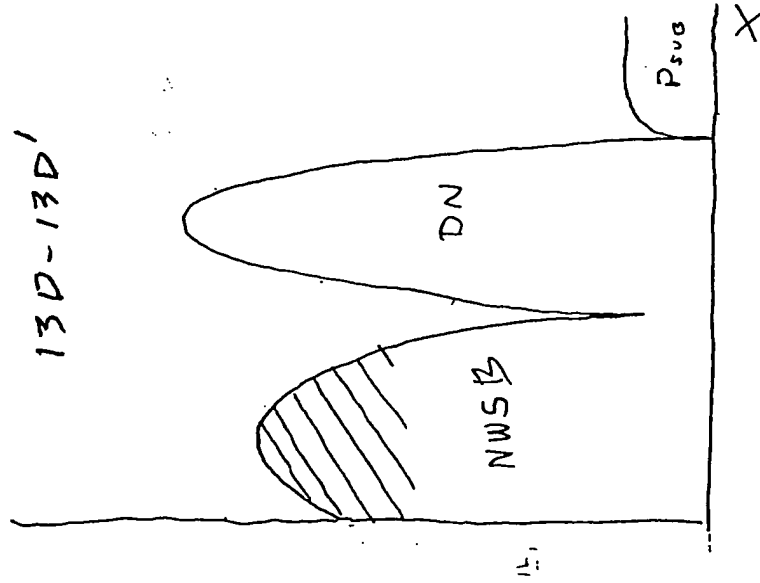


Fig. 13H

13D-13D'



41/219

Fig. 13E

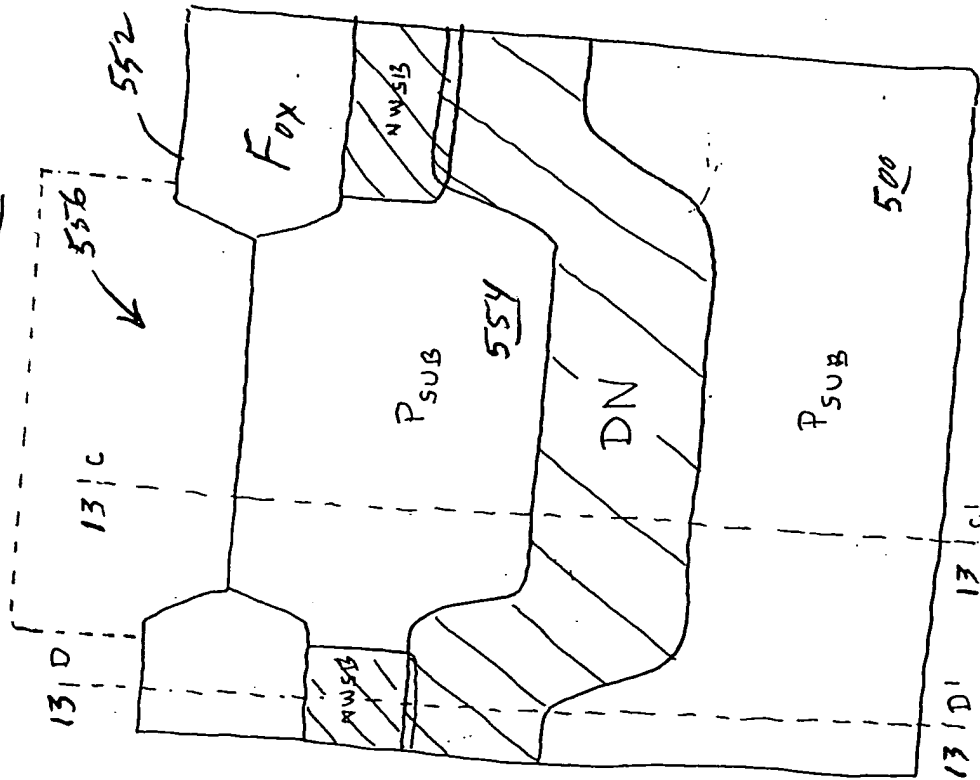


Fig. 13F

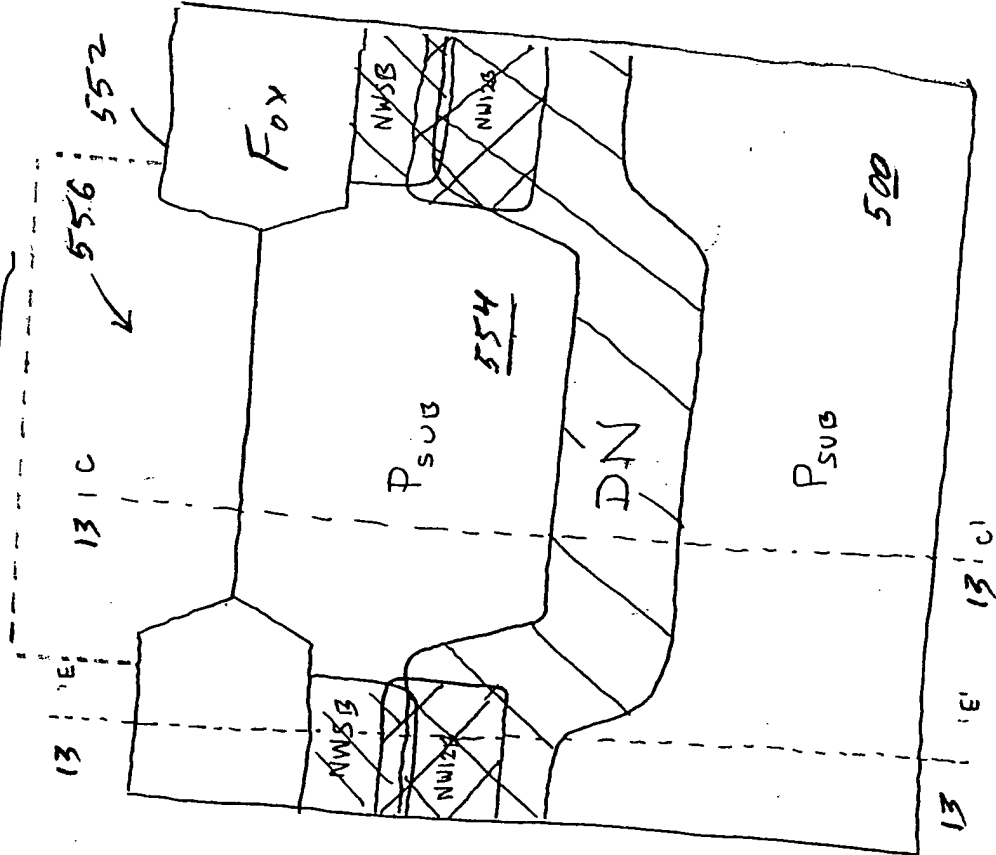


Fig. 13I

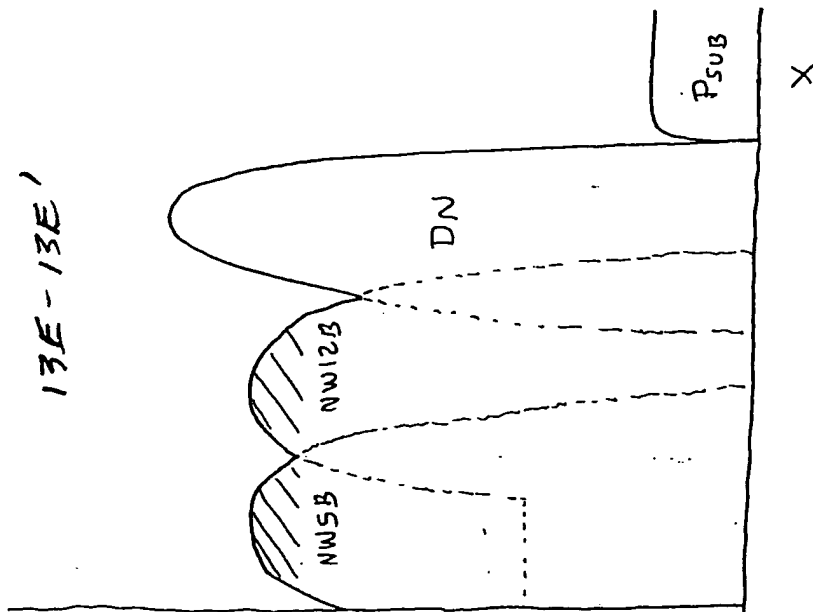


Fig 14A

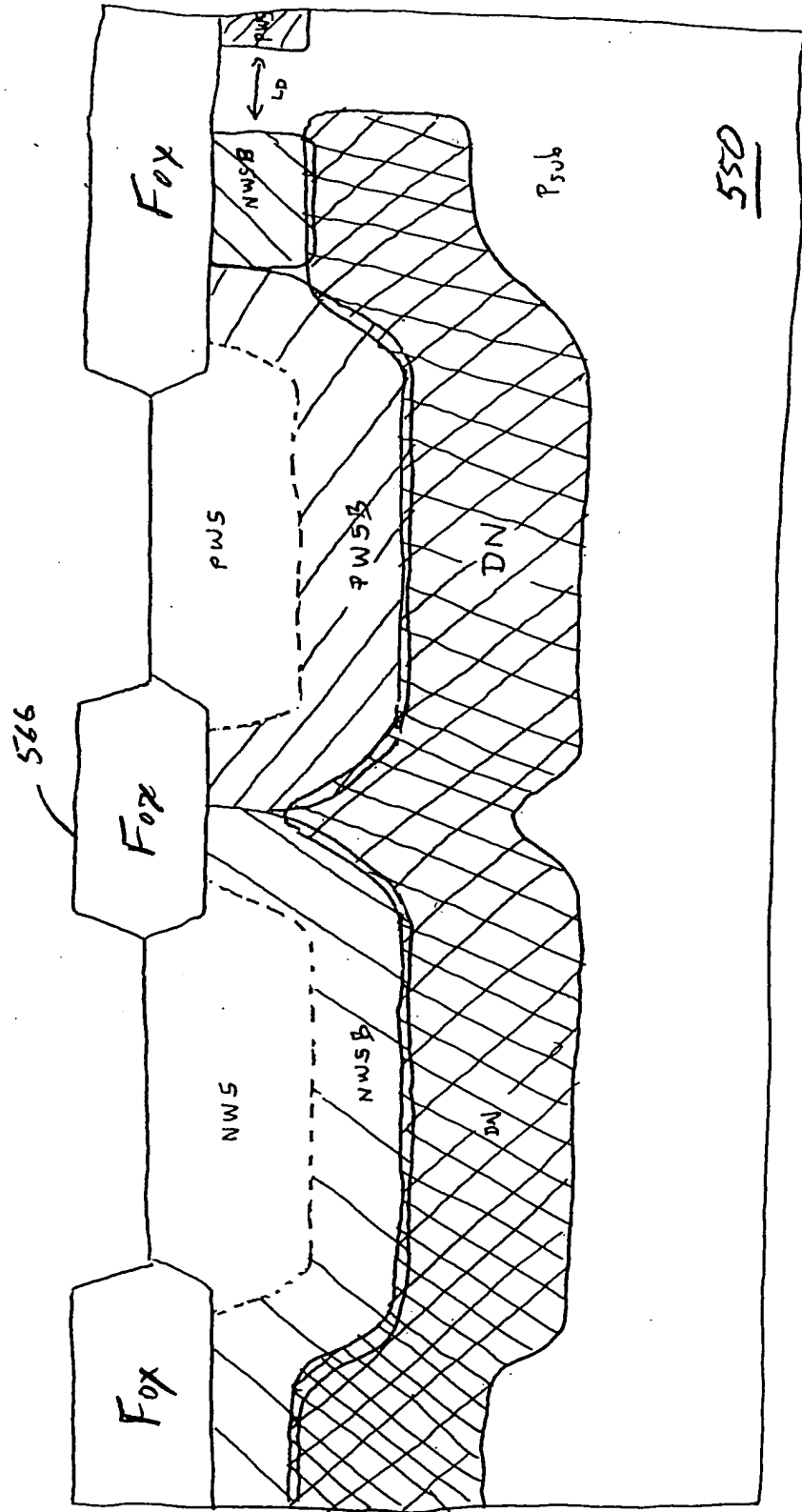


Fig. 14B

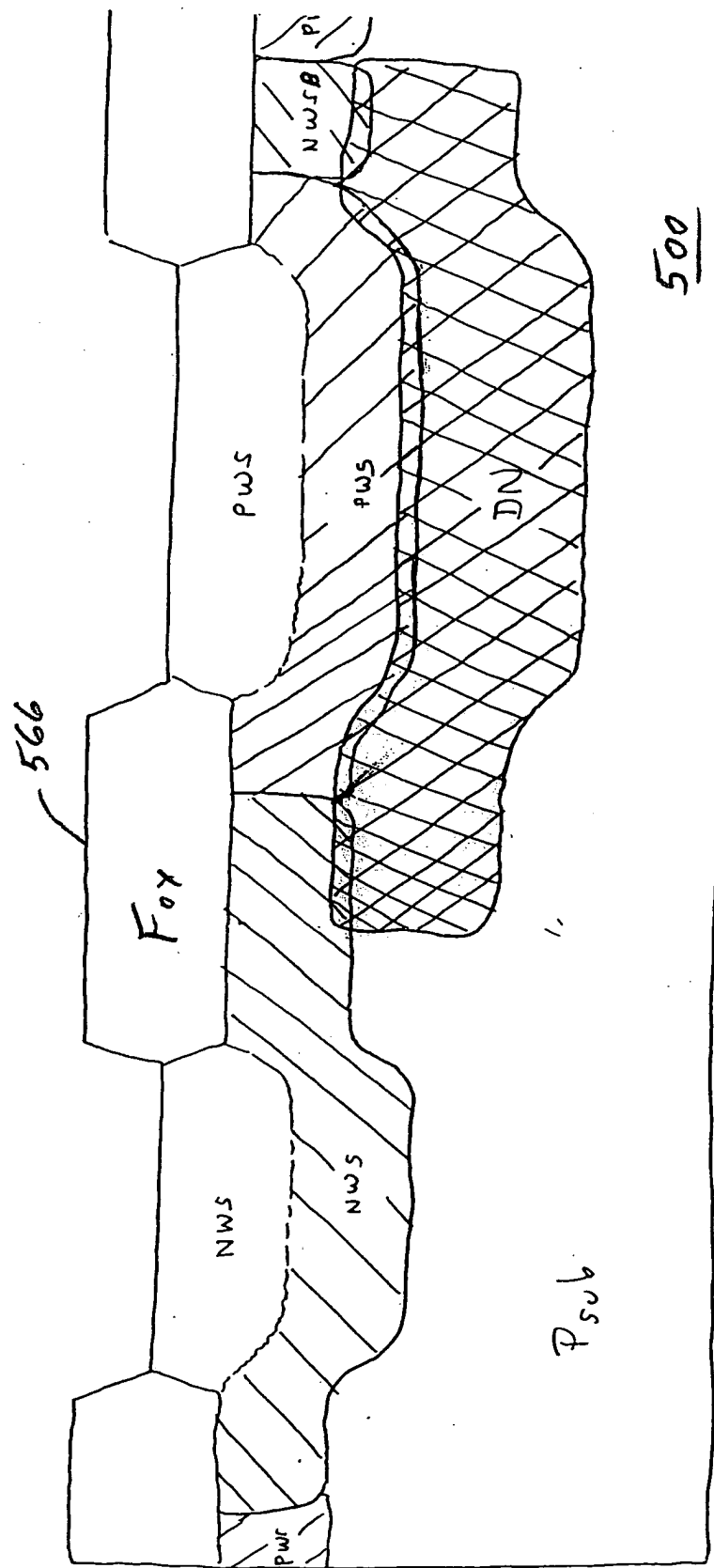
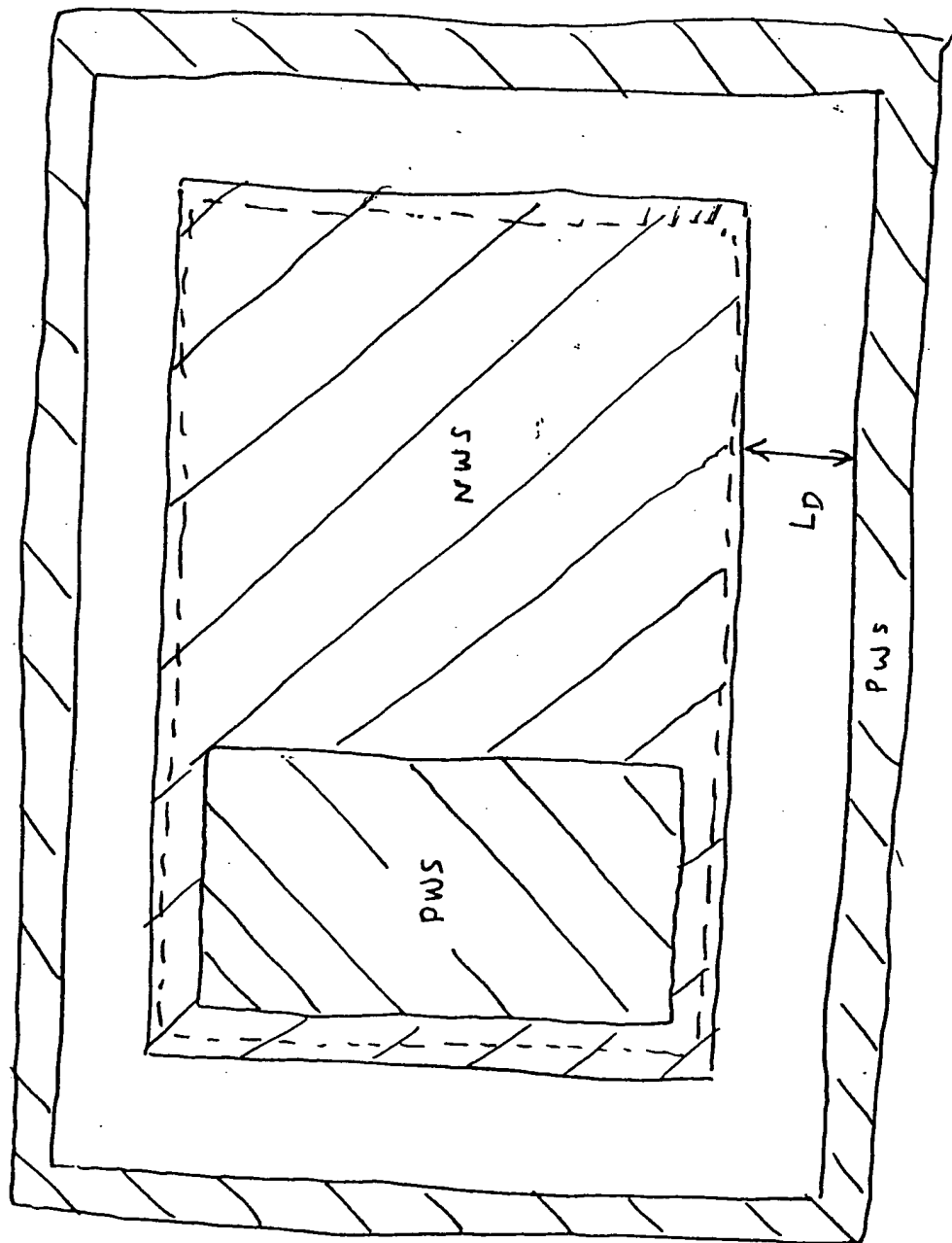


Fig. 14 C



45/219

46/219

Fig 14D

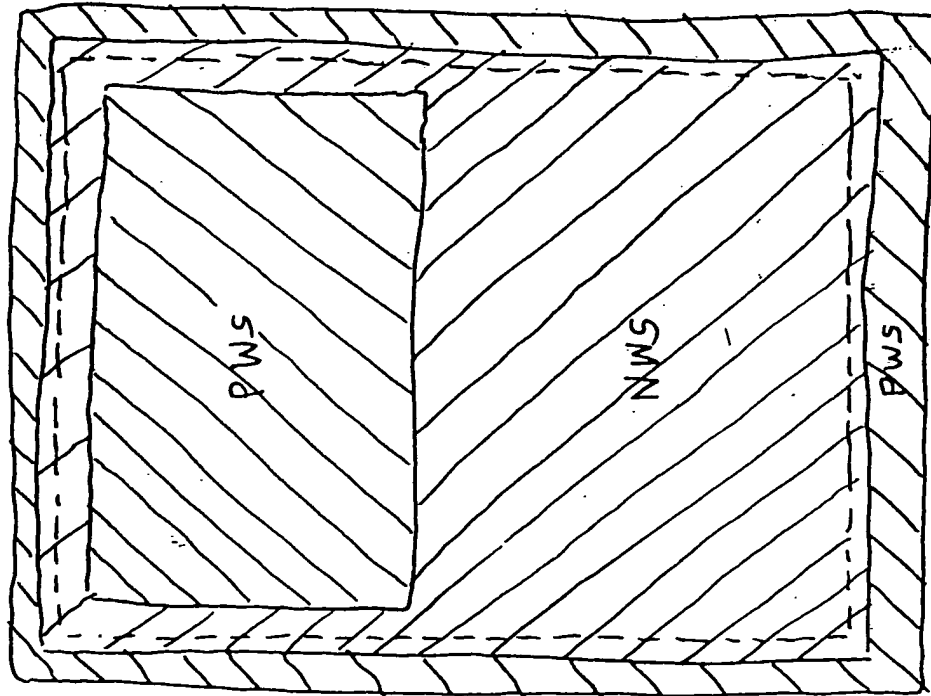
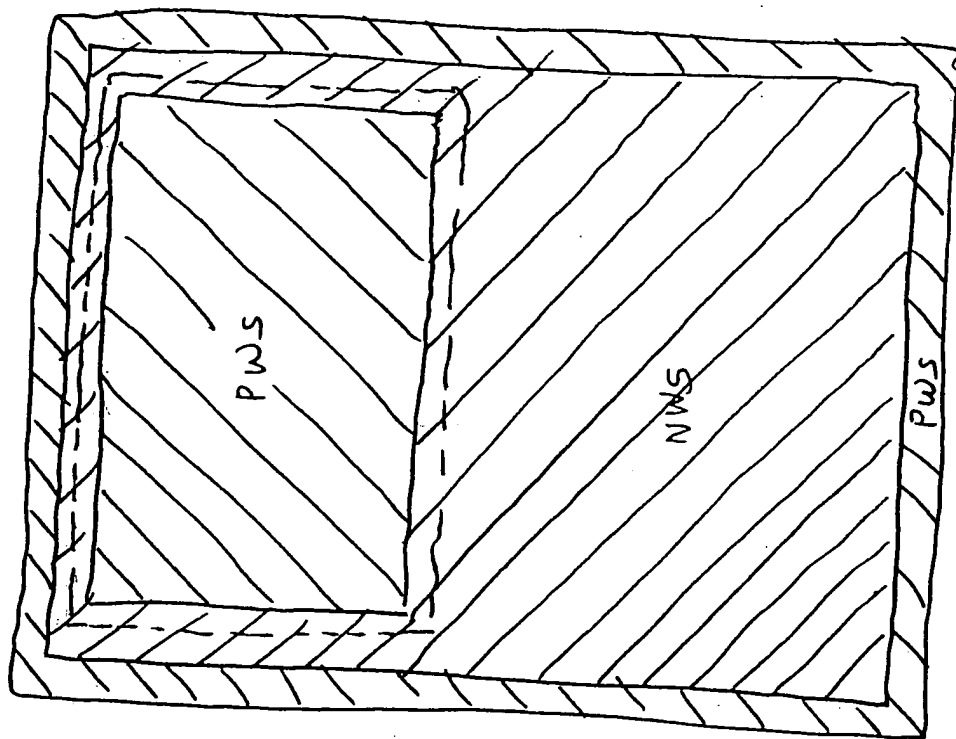


Fig. 14E



48/219

Fig. 146

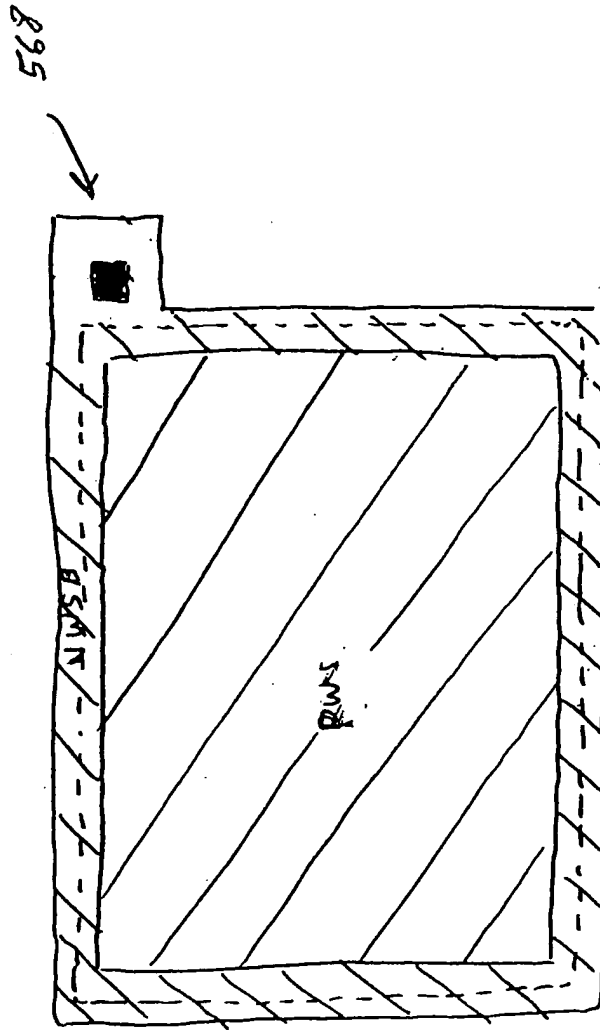


Fig. 14H

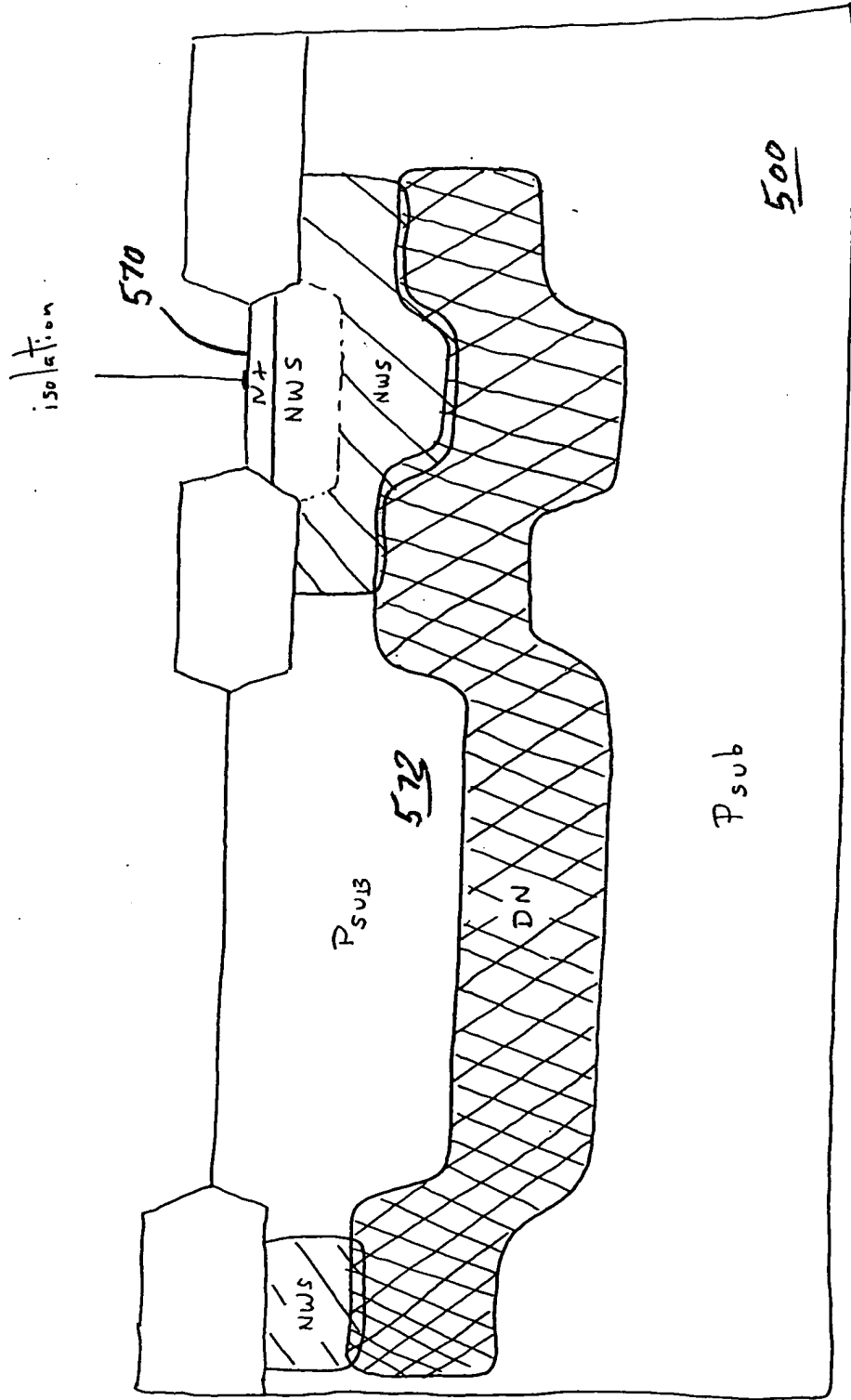


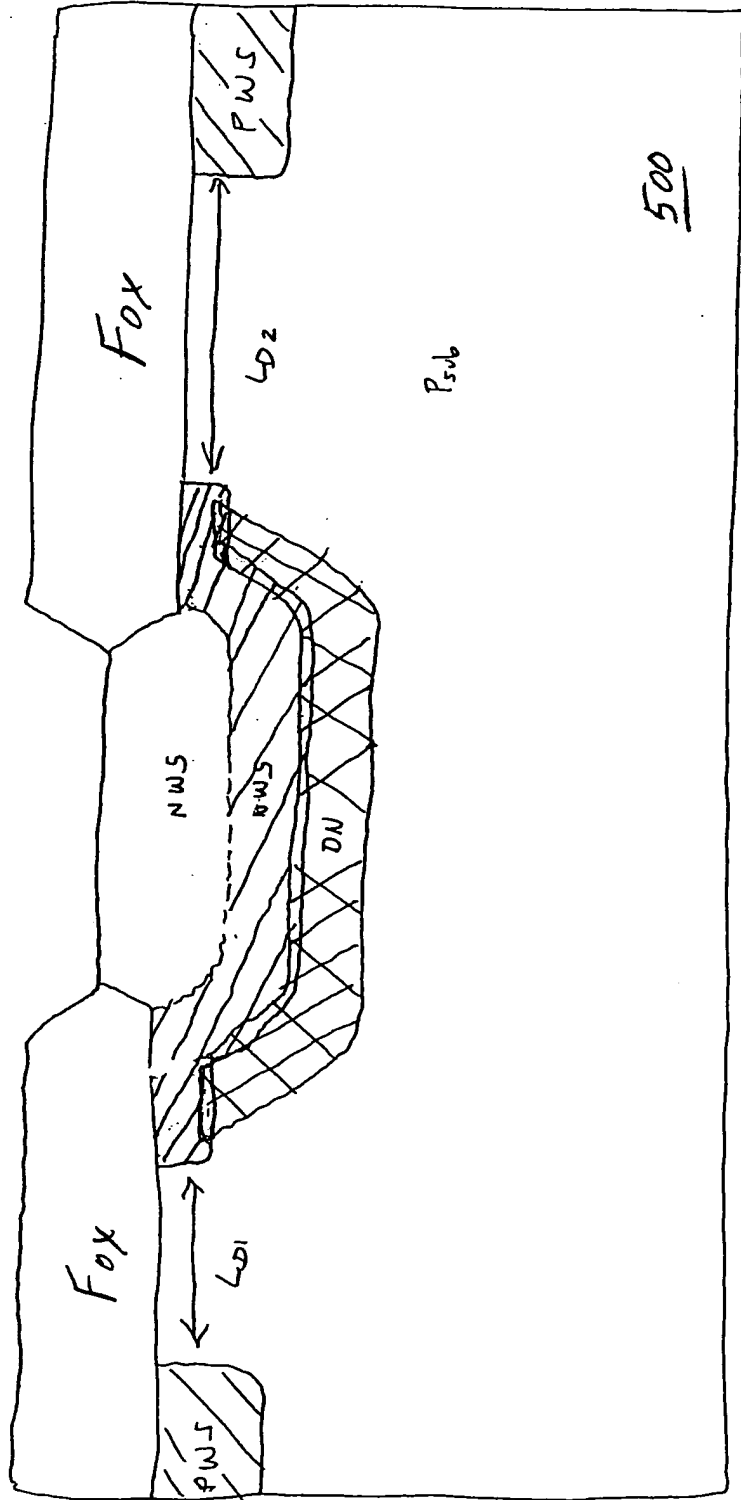
Fig. 14I.

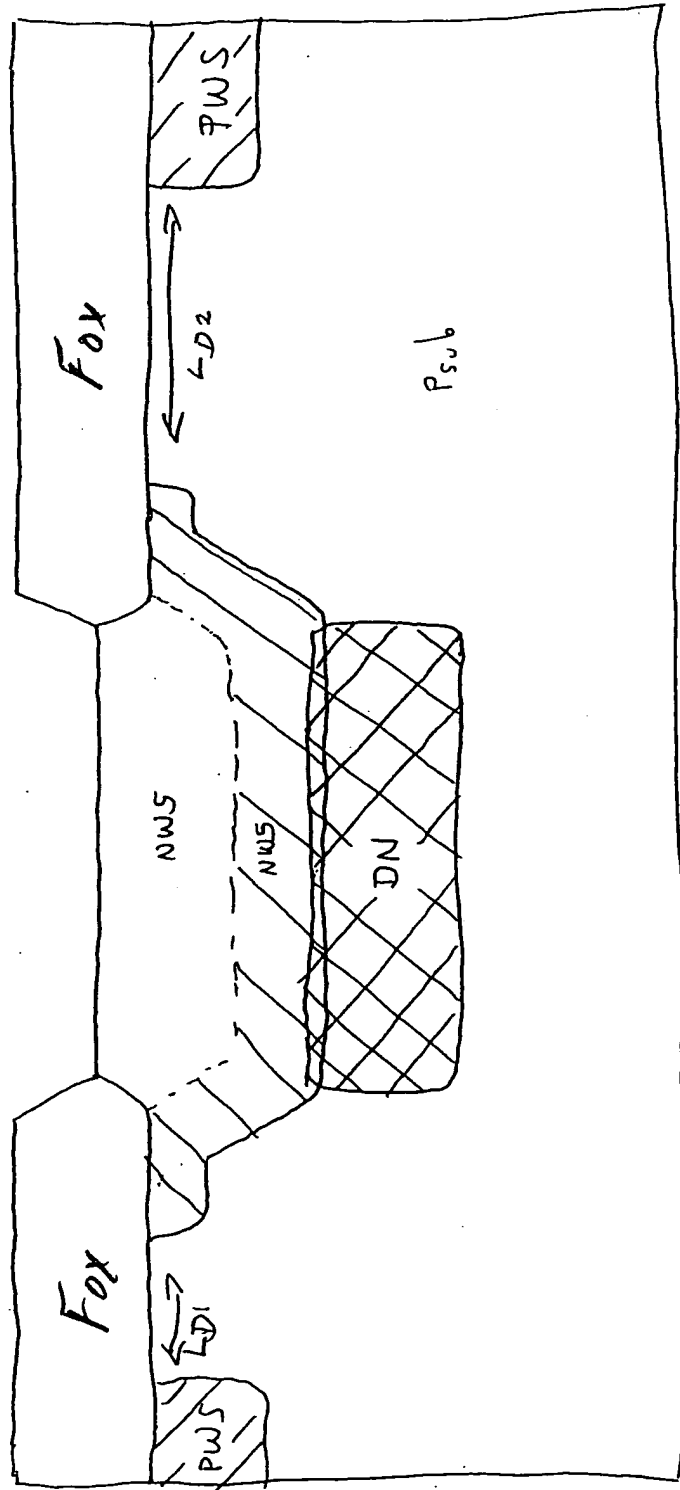
Fig. 14J

Fig. 14K

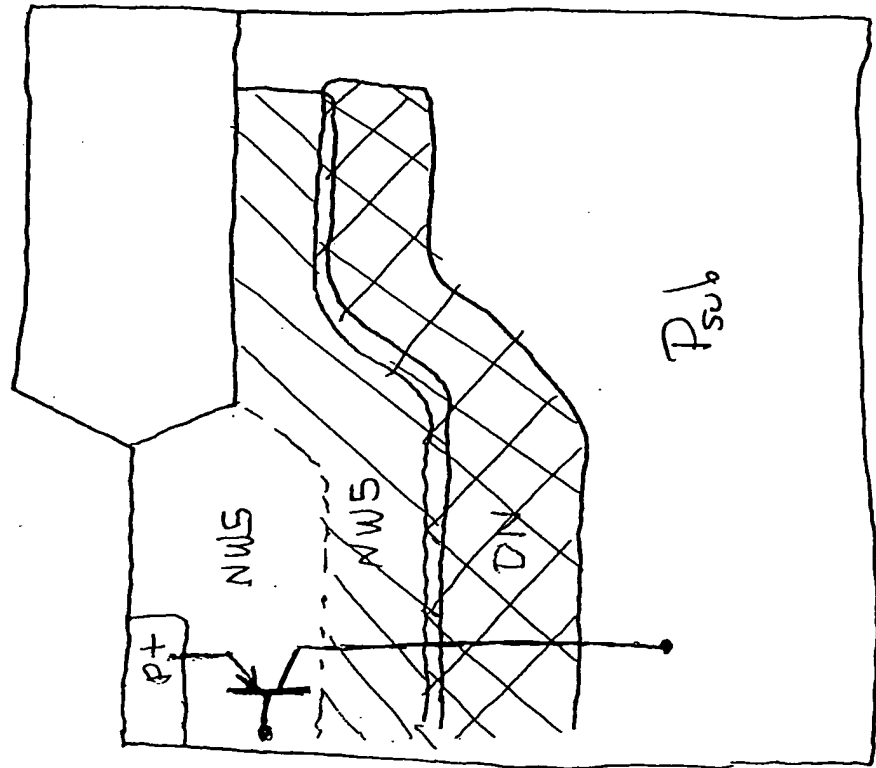


Fig. 14L

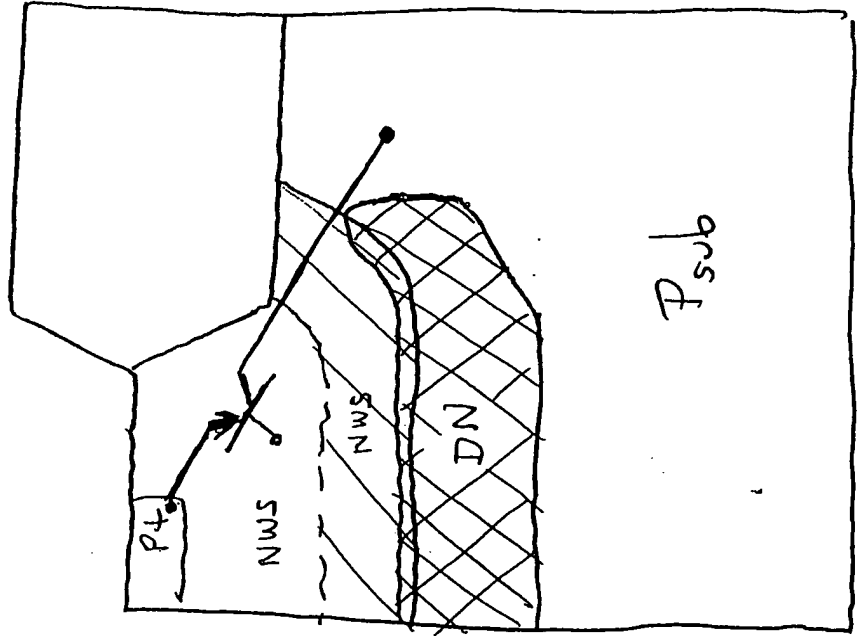


Fig. 14RM

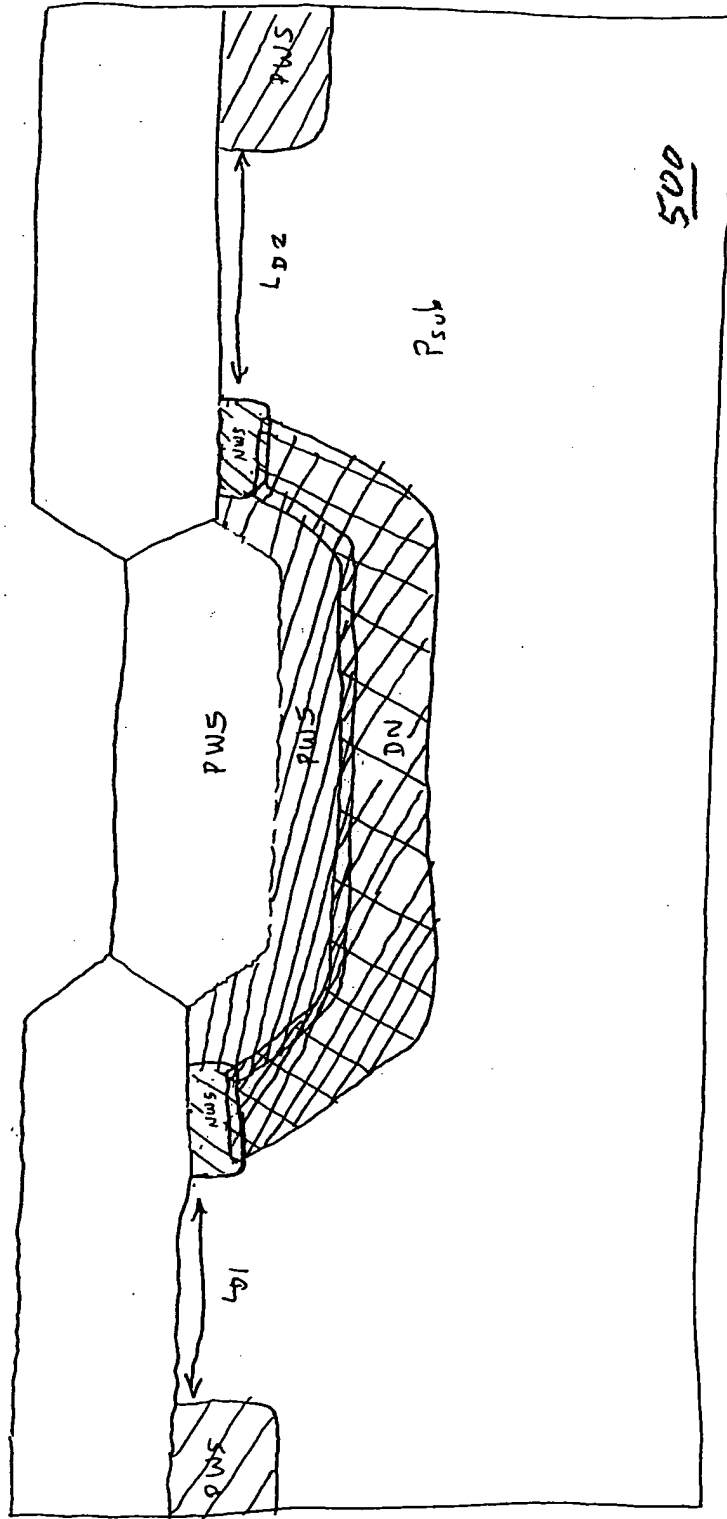


Fig. 14N

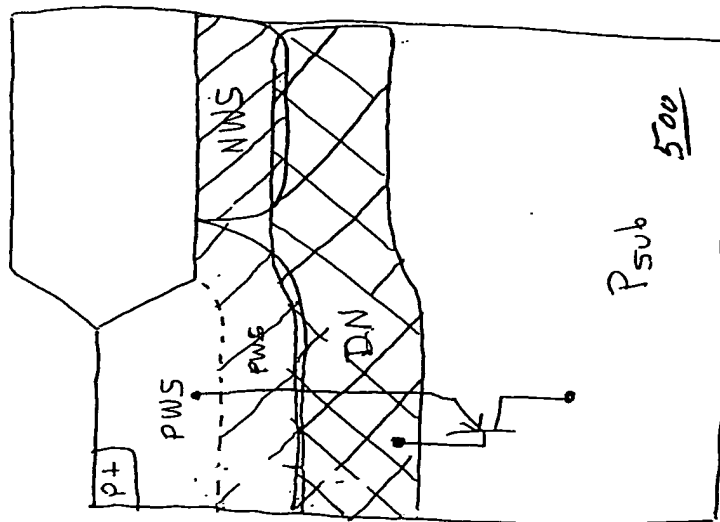


Fig. 14O

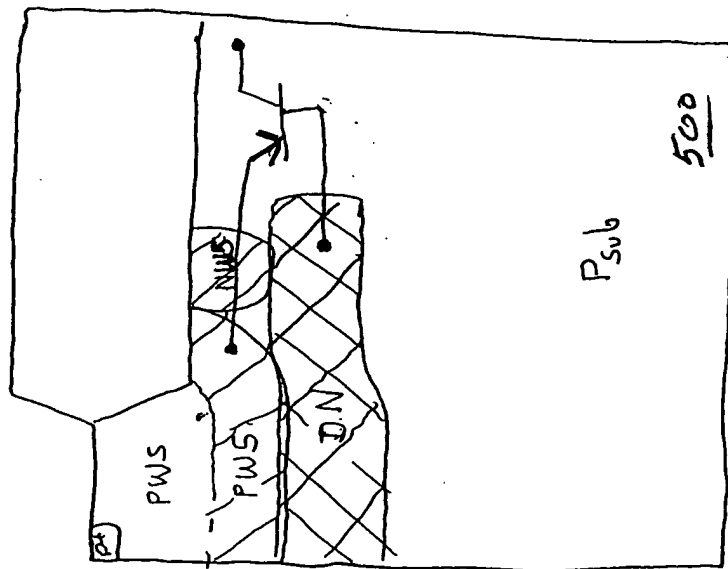


Fig. 14P

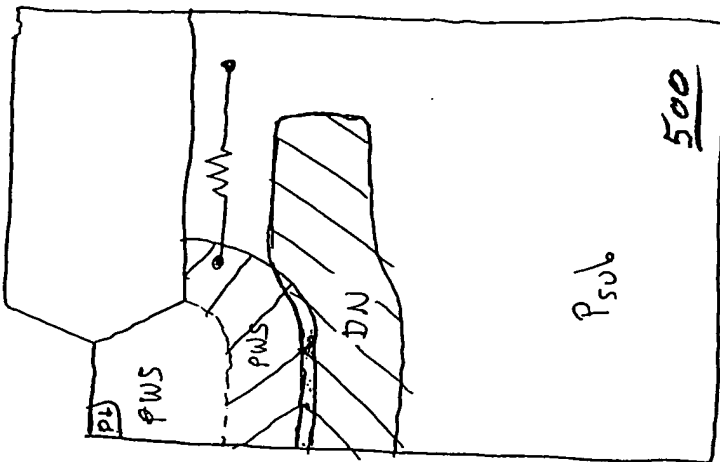


Fig. 15A

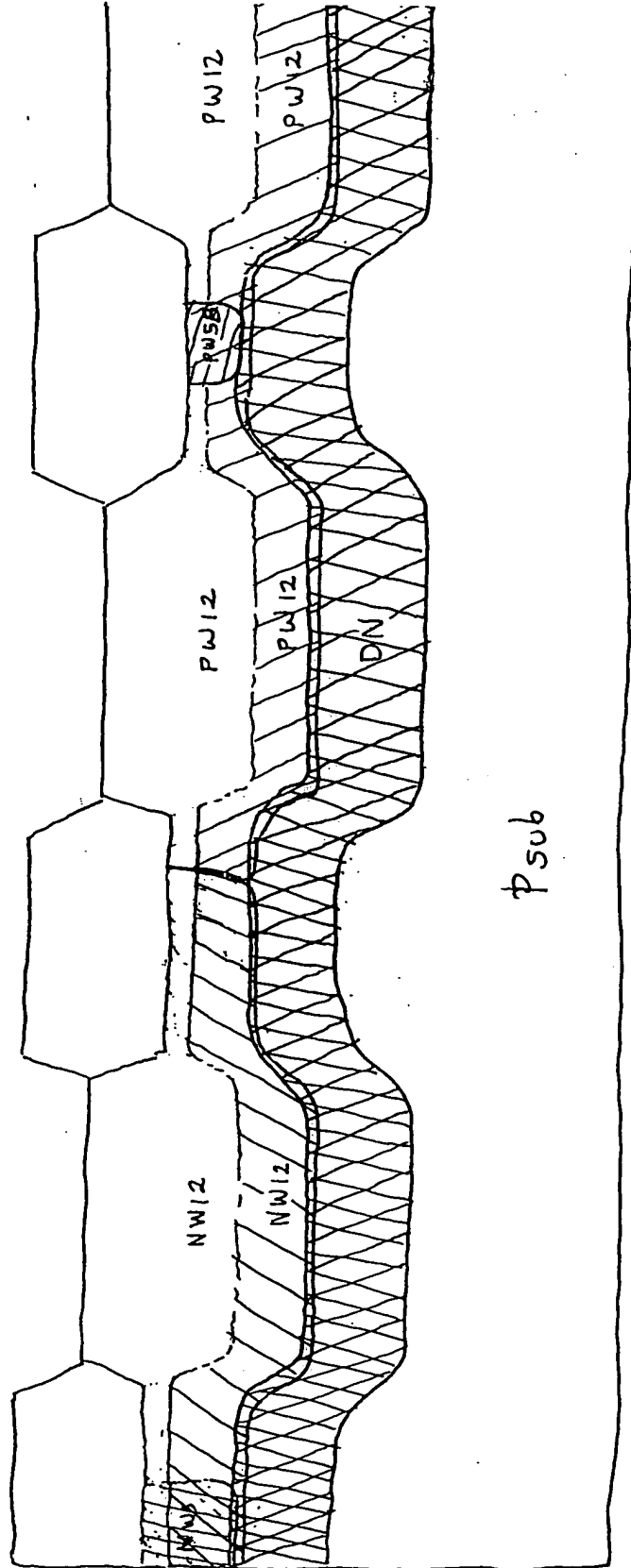


Fig. 15B

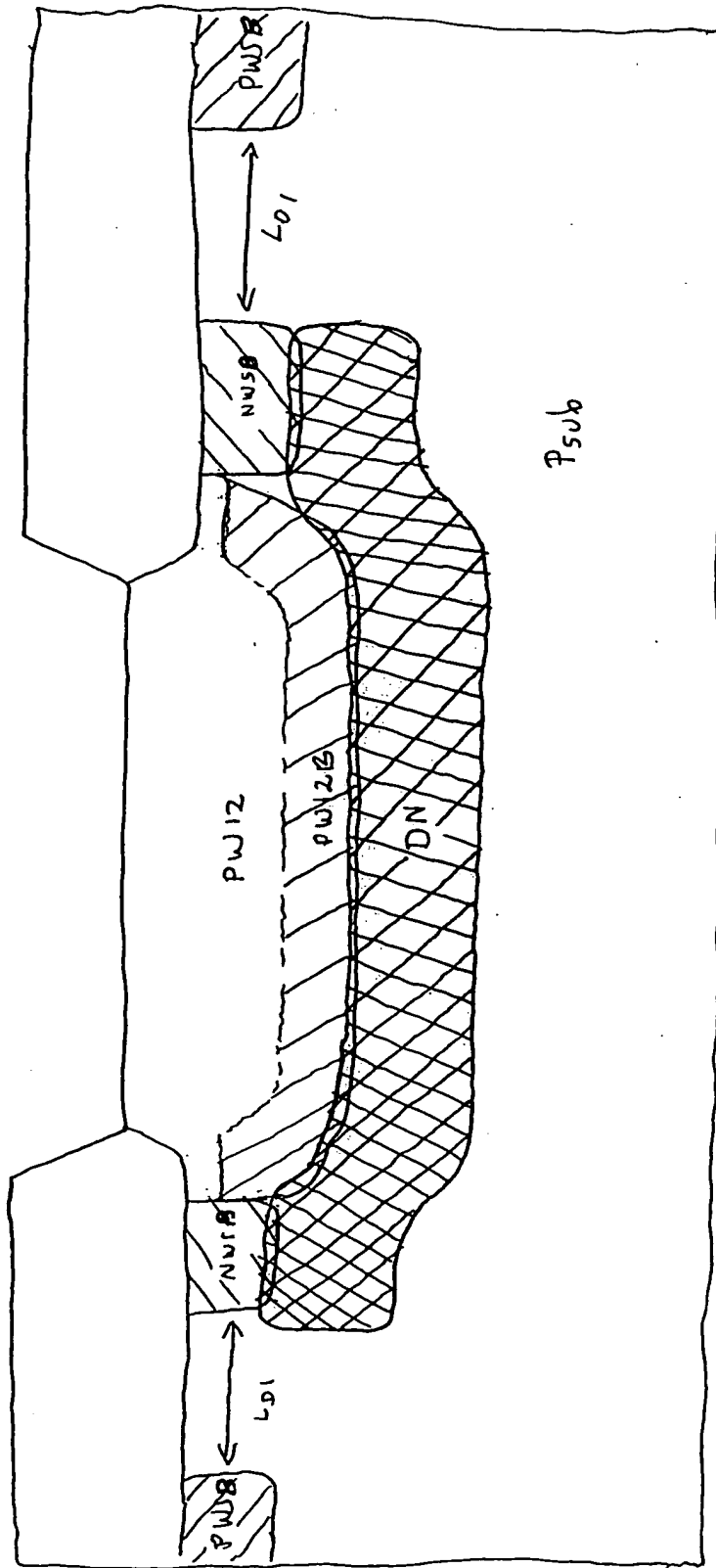


Fig. 15C

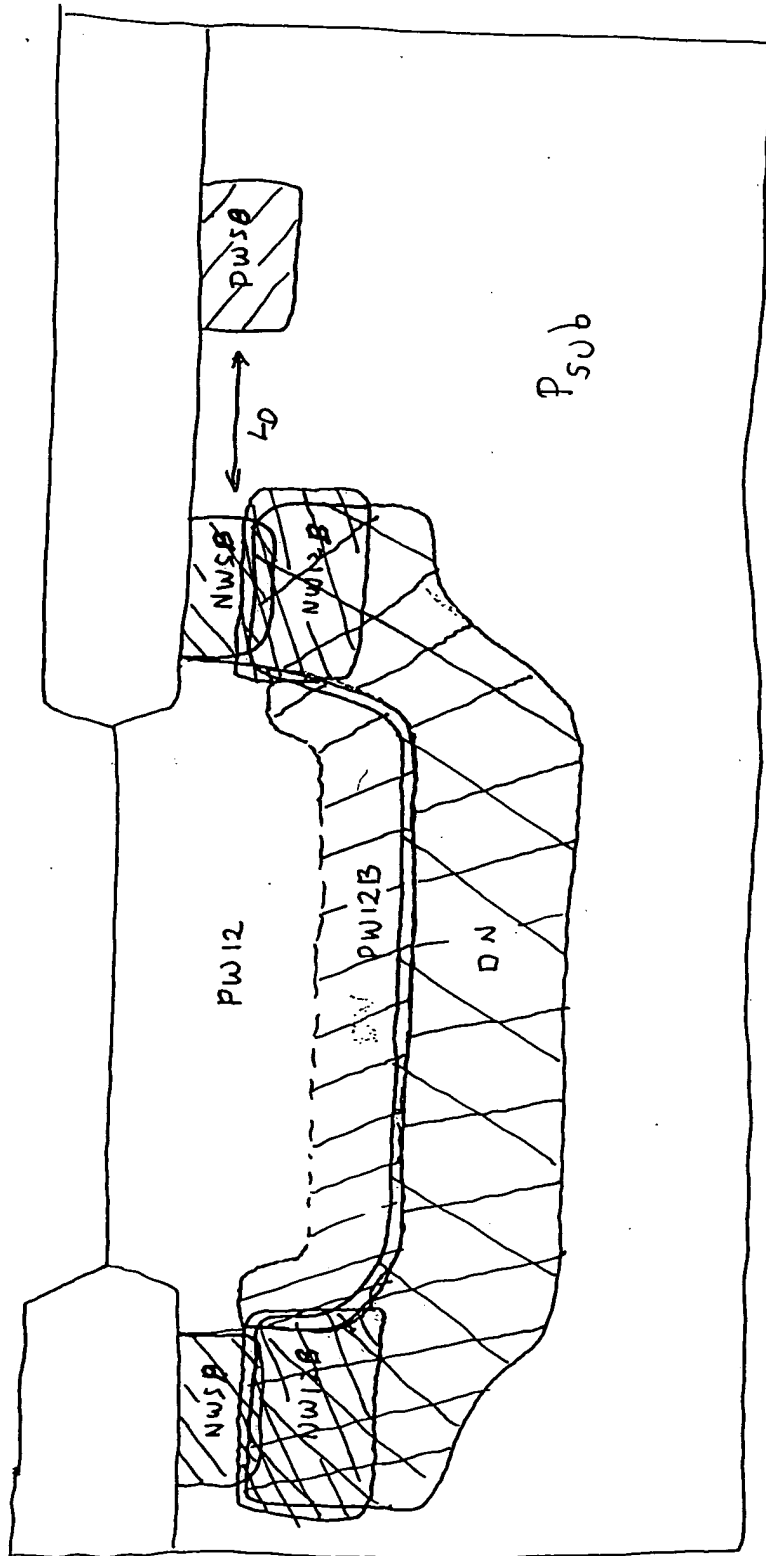


Fig. 15D

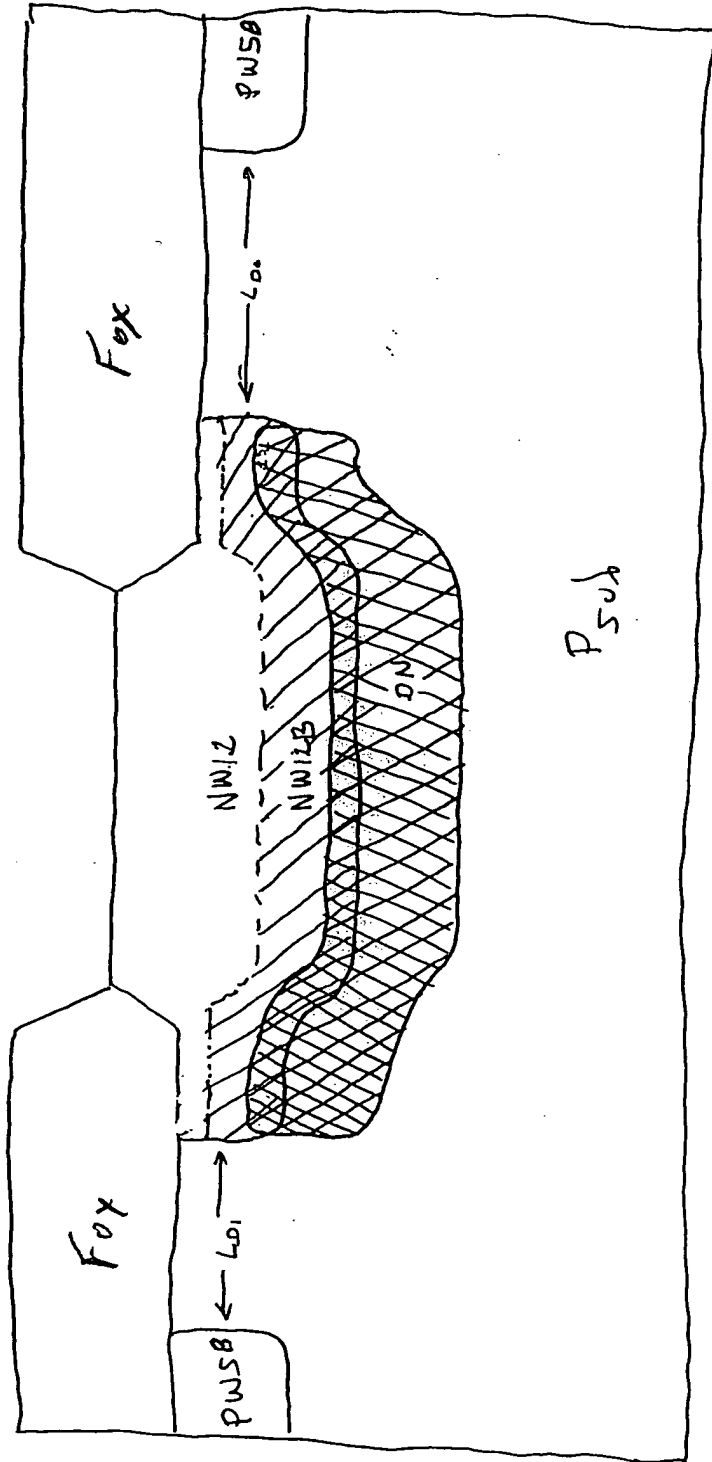


Fig. 15E

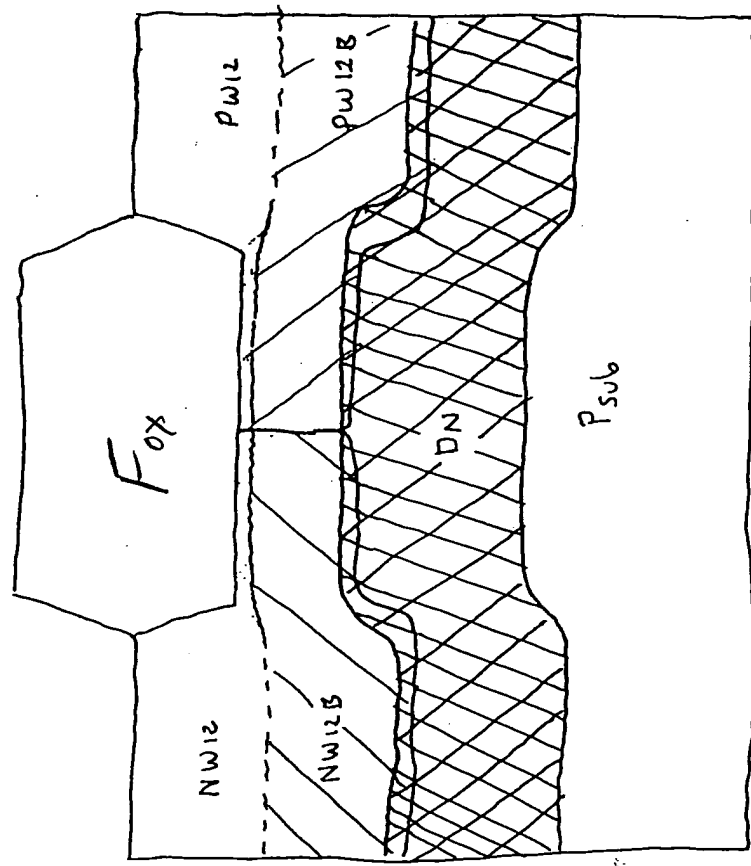
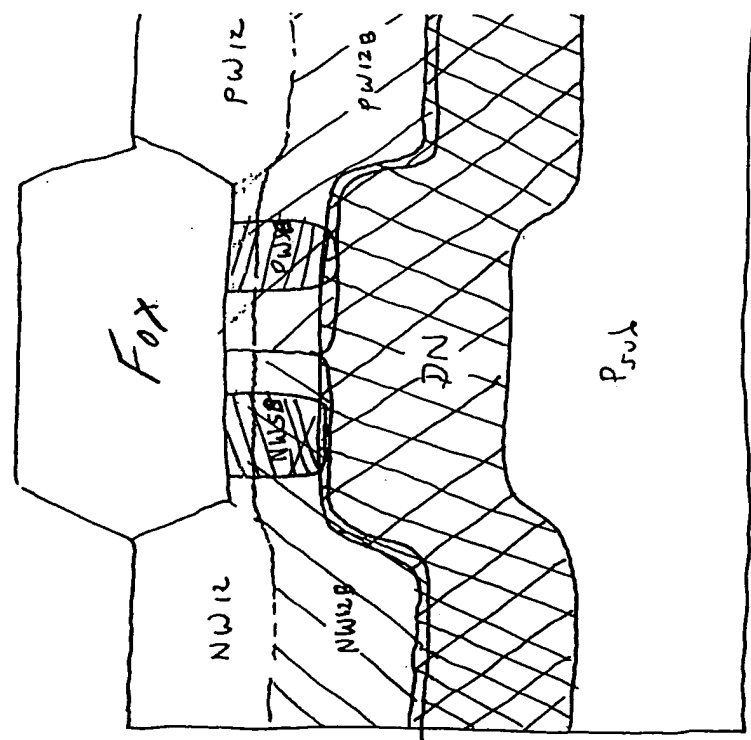


Fig. 15F



61/219

Fig. 16B

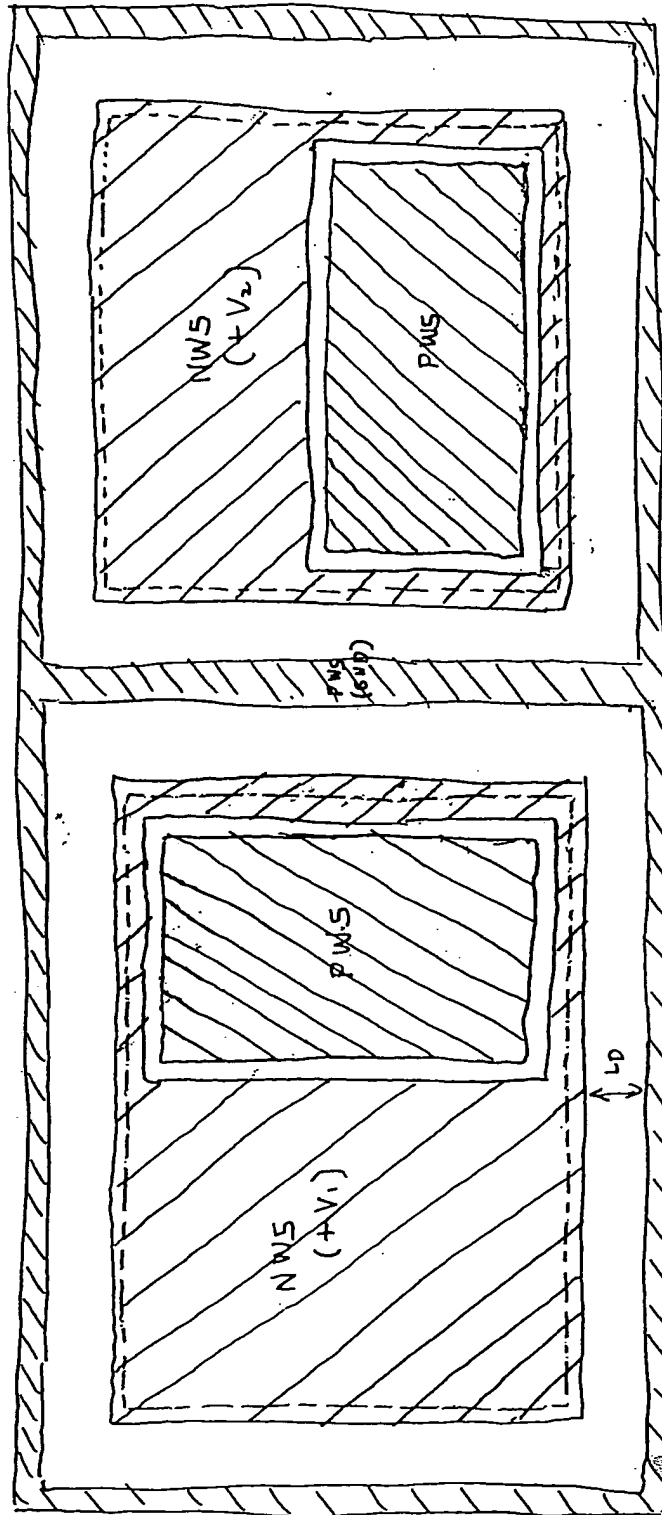
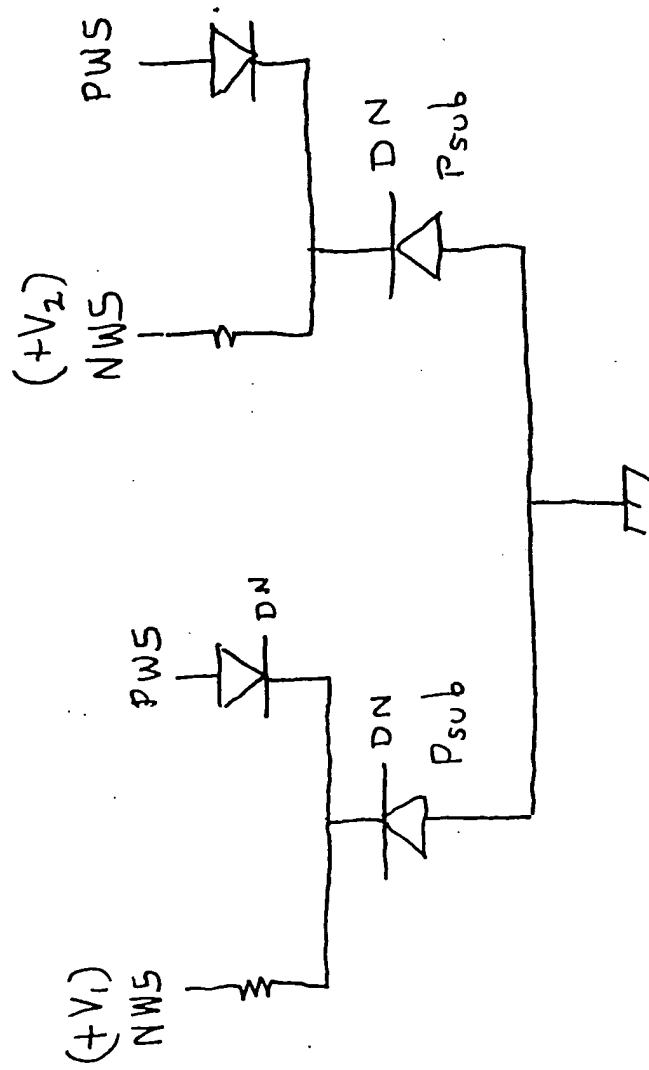


Fig. 16C



63/219

Fig. 16D

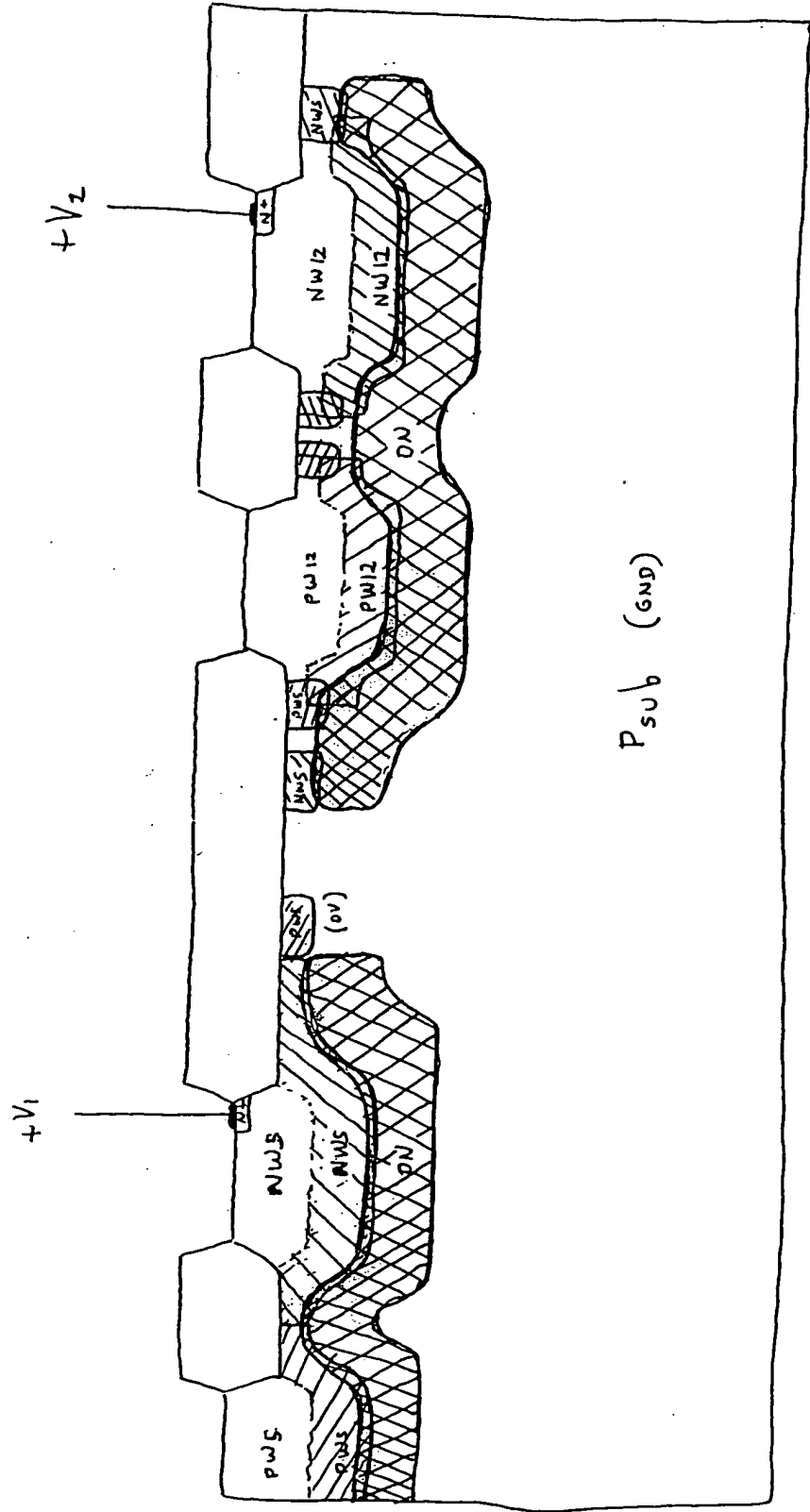
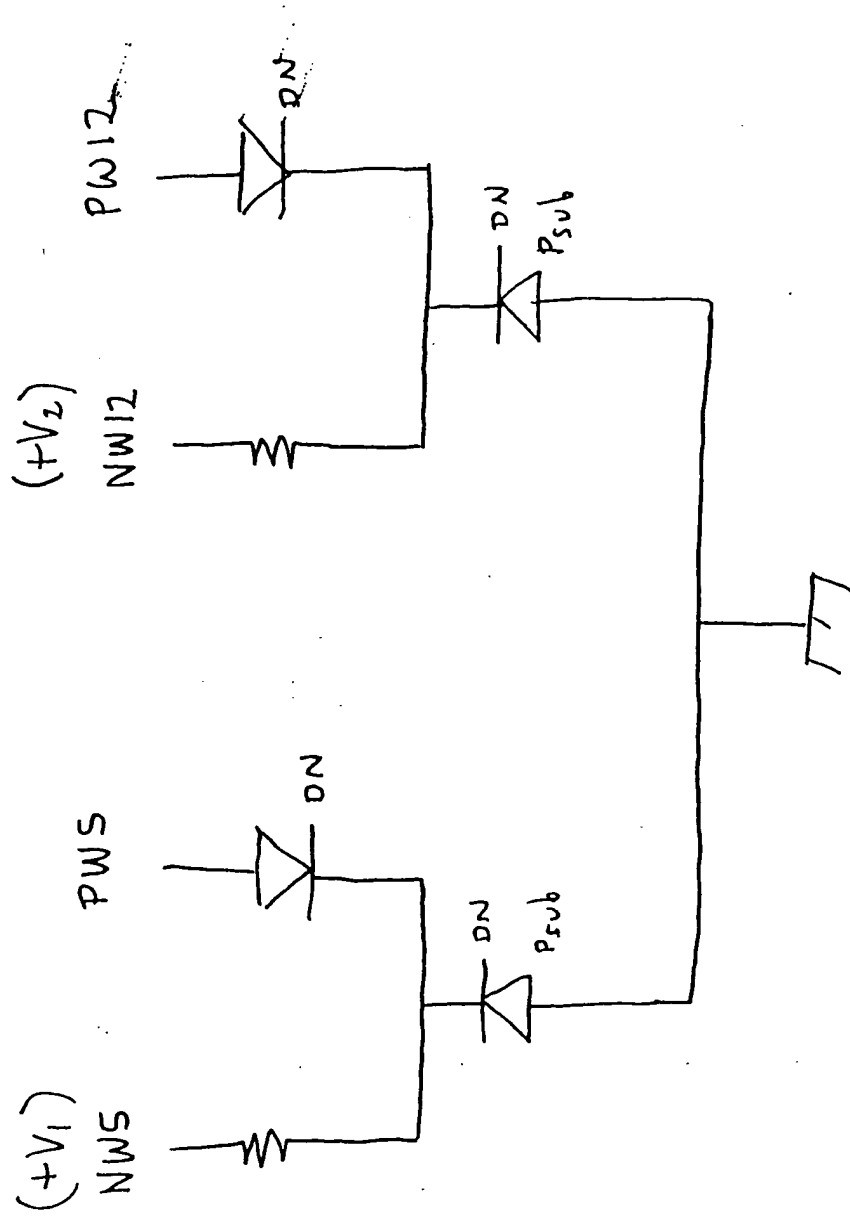


Fig. 16E

65/219

Fig. 16F

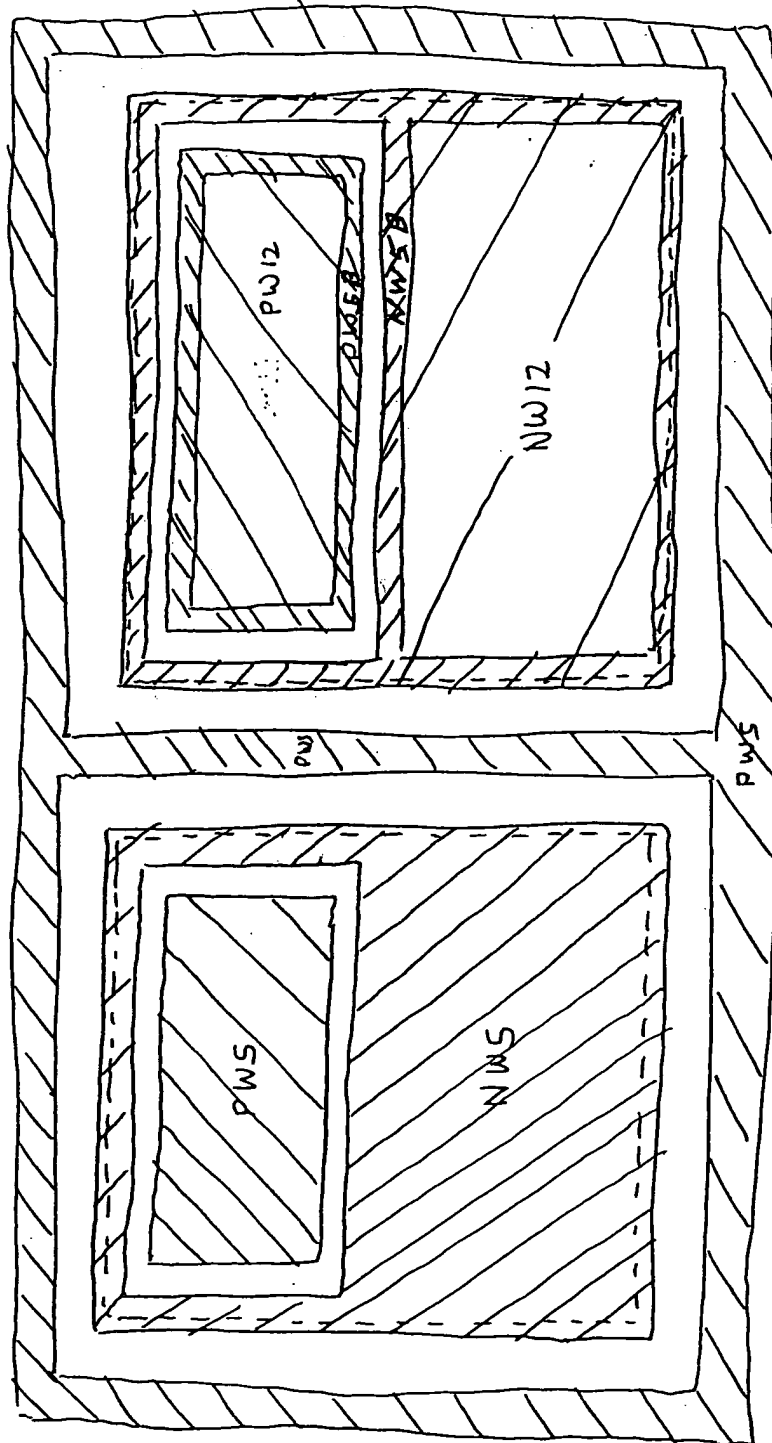


Fig. 17A

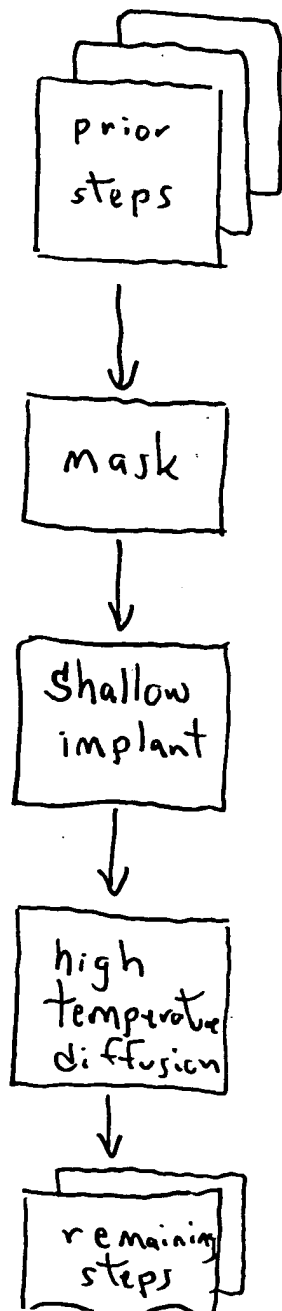
Prior Art

Fig. 17B

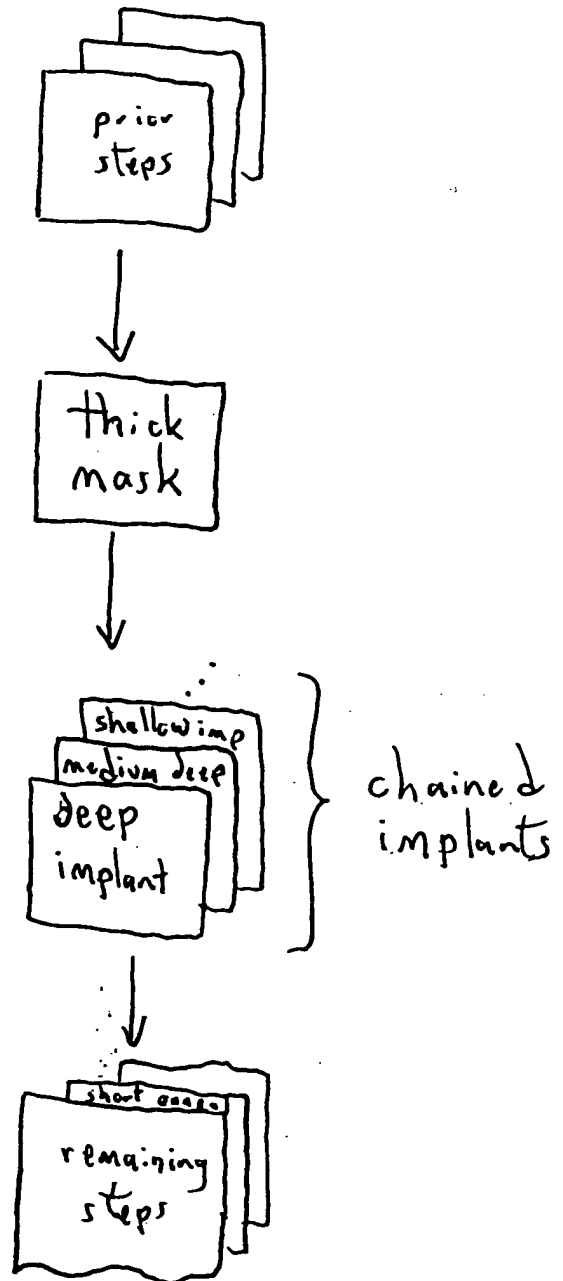


Fig. 17C

Prior Art

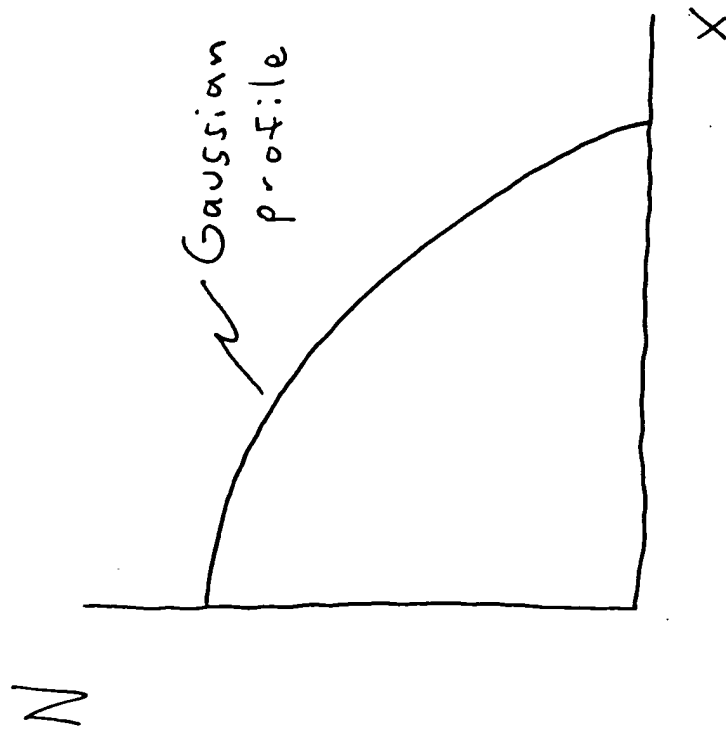


Fig. 17D

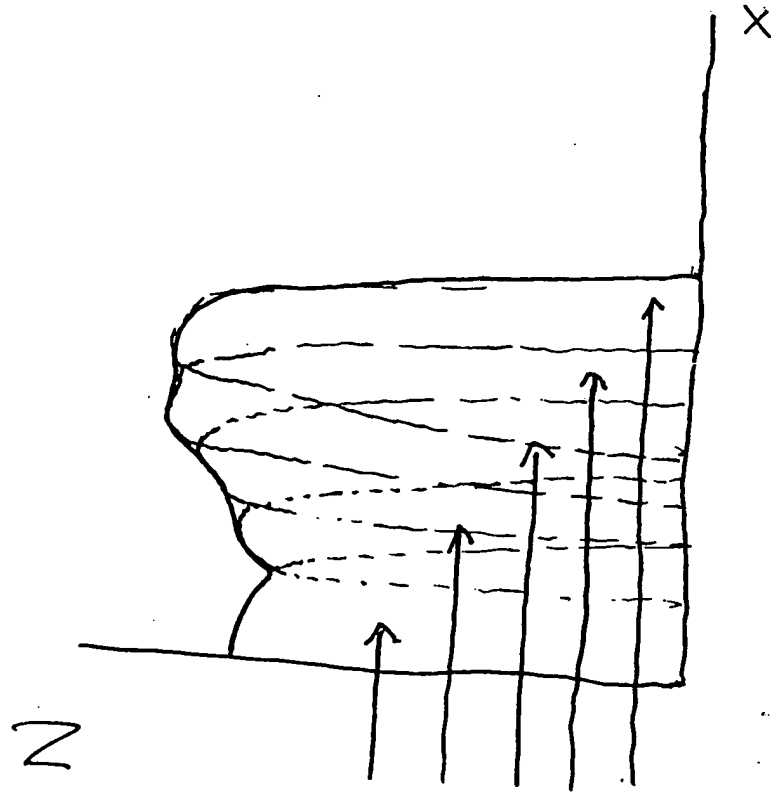


Fig. 17E

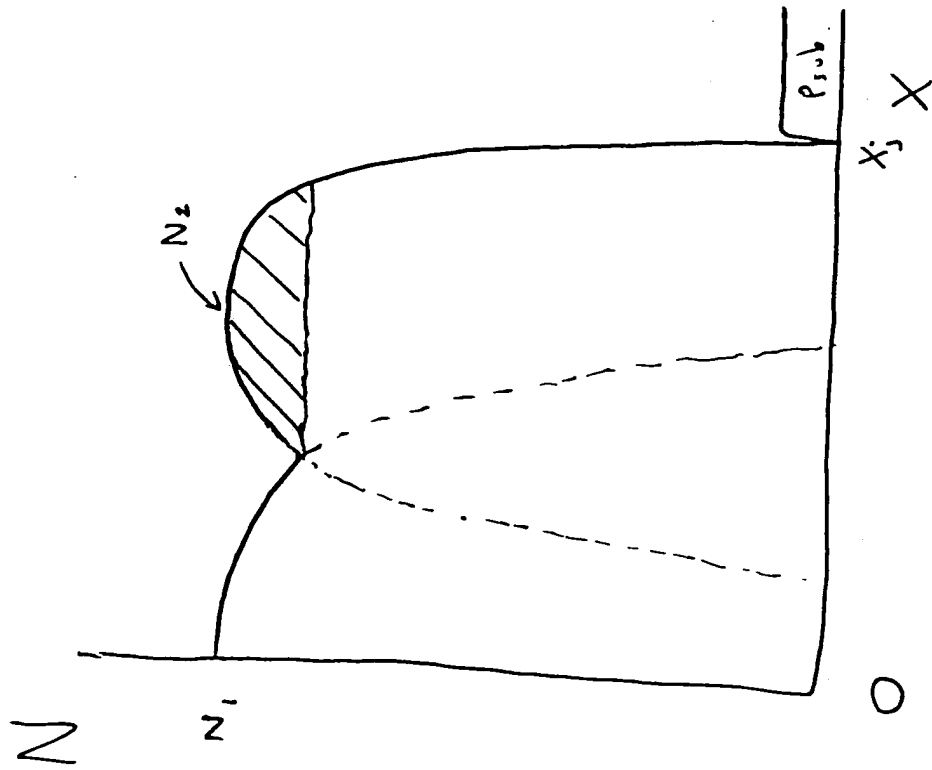


Fig. 17F

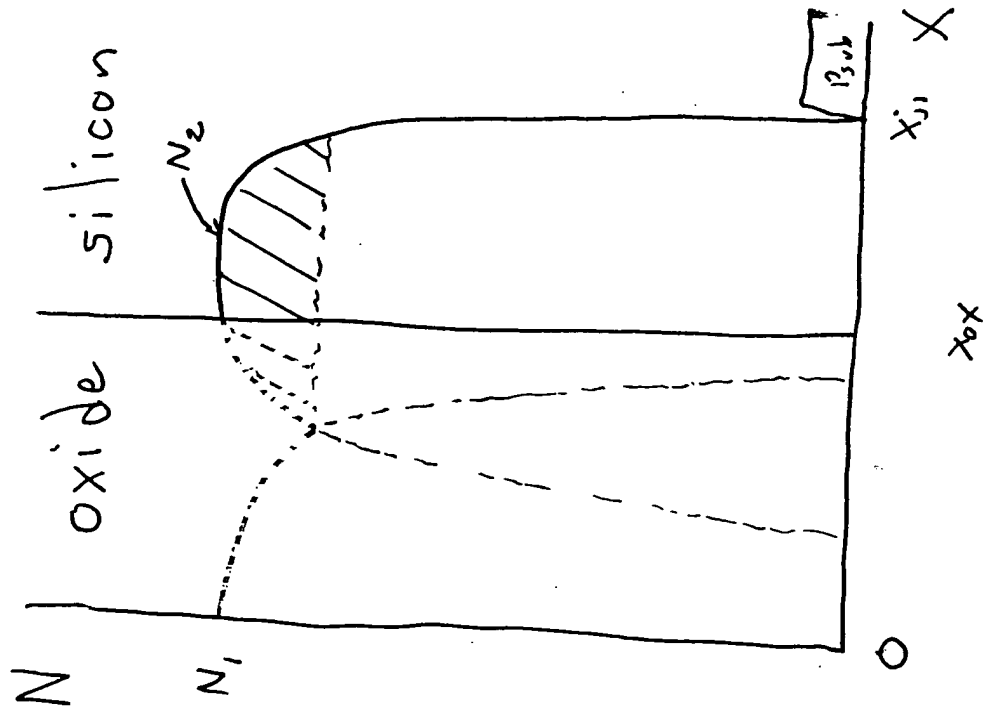


Fig. 176

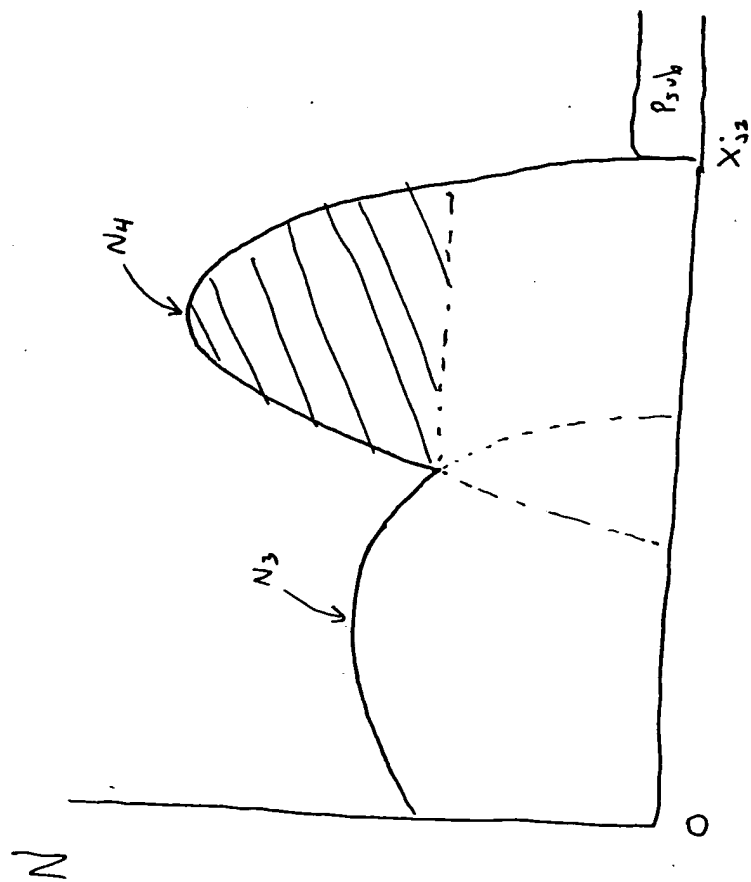


Fig. 17H

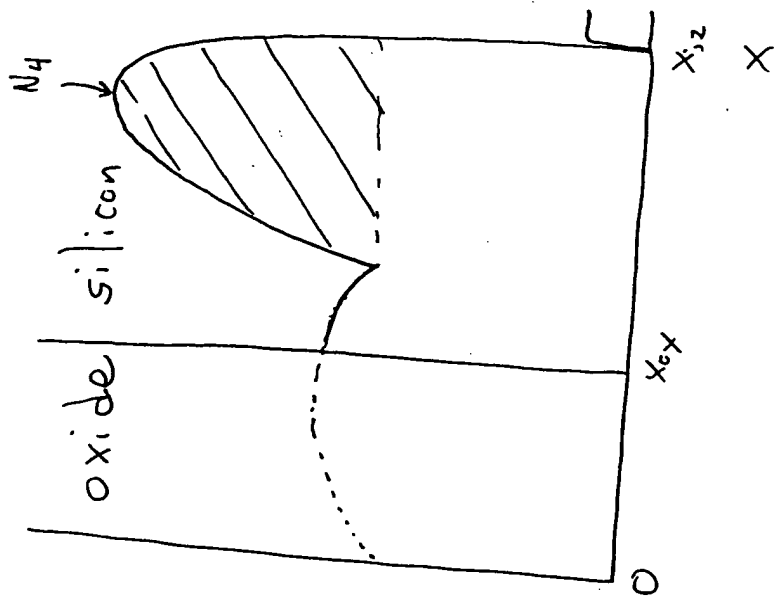


Fig. 17I

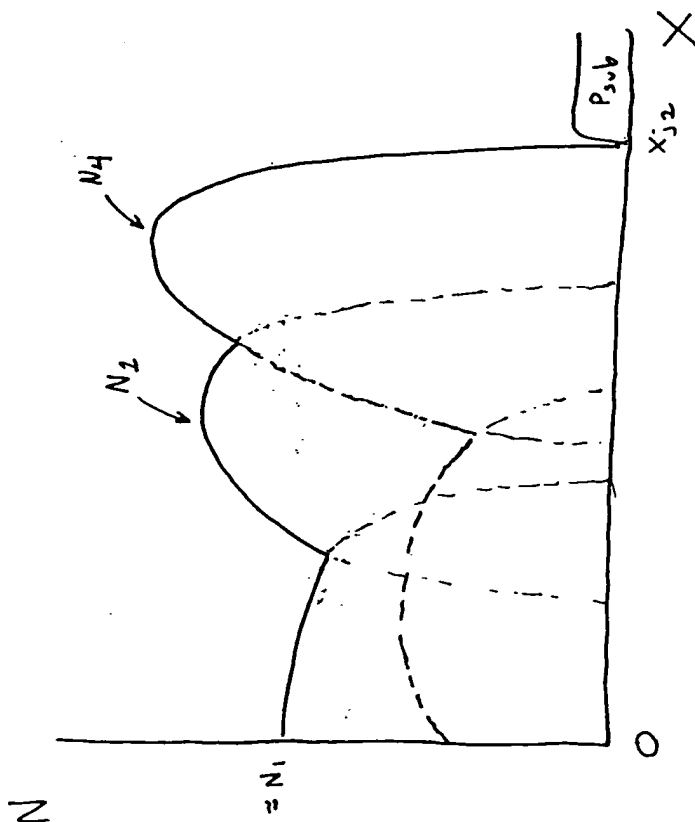
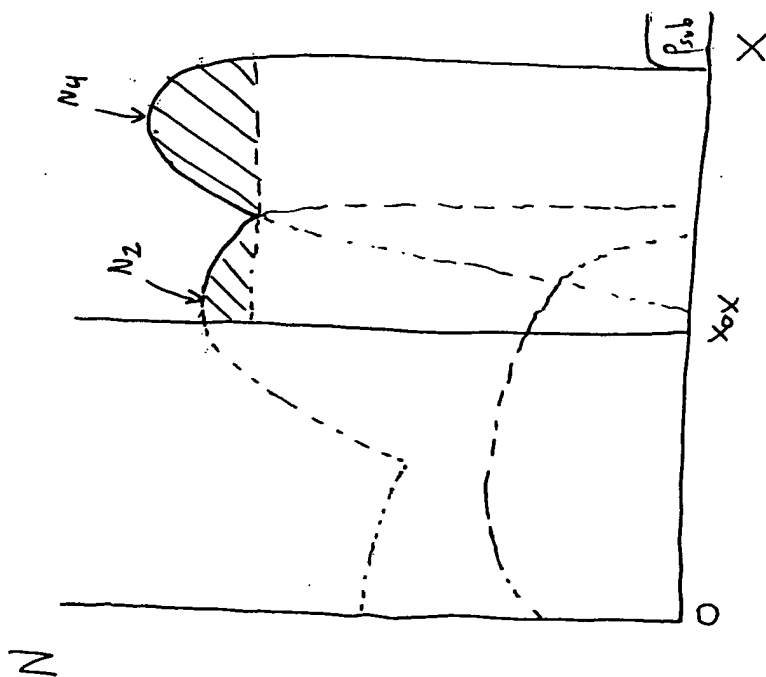


Fig. 17J



7/1/219

Fig. 17K
Prior Art

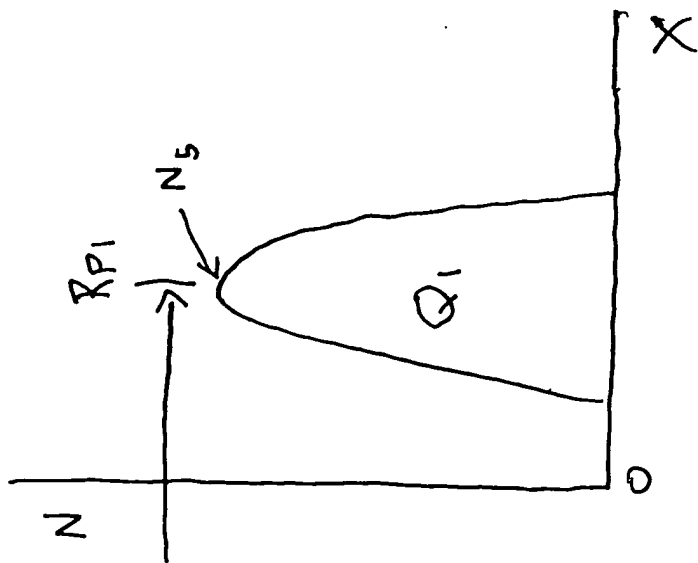


Fig. 17L
Prior Art

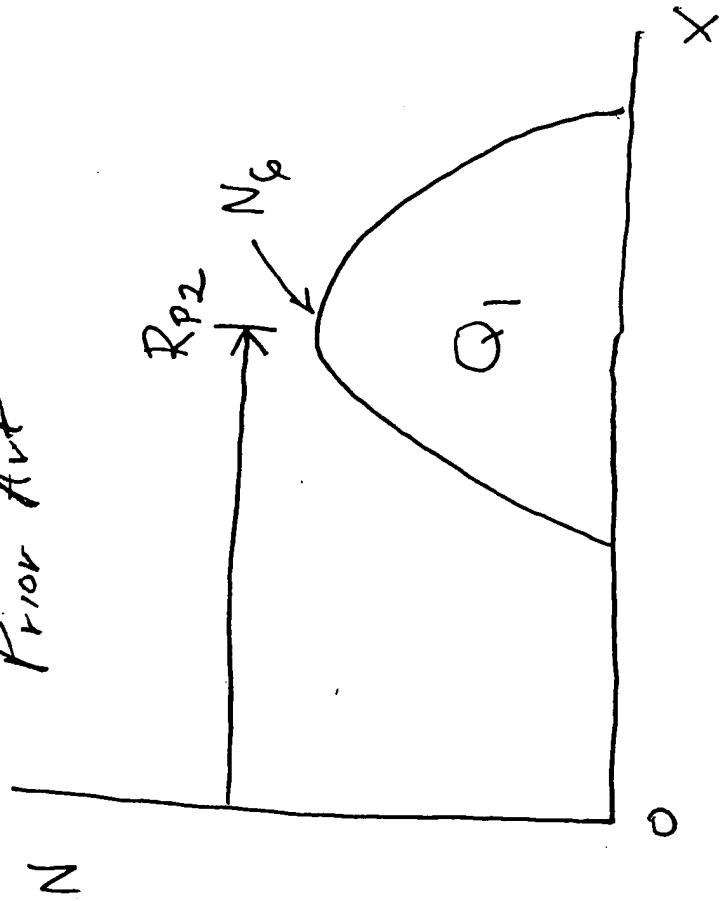


Fig. 17M

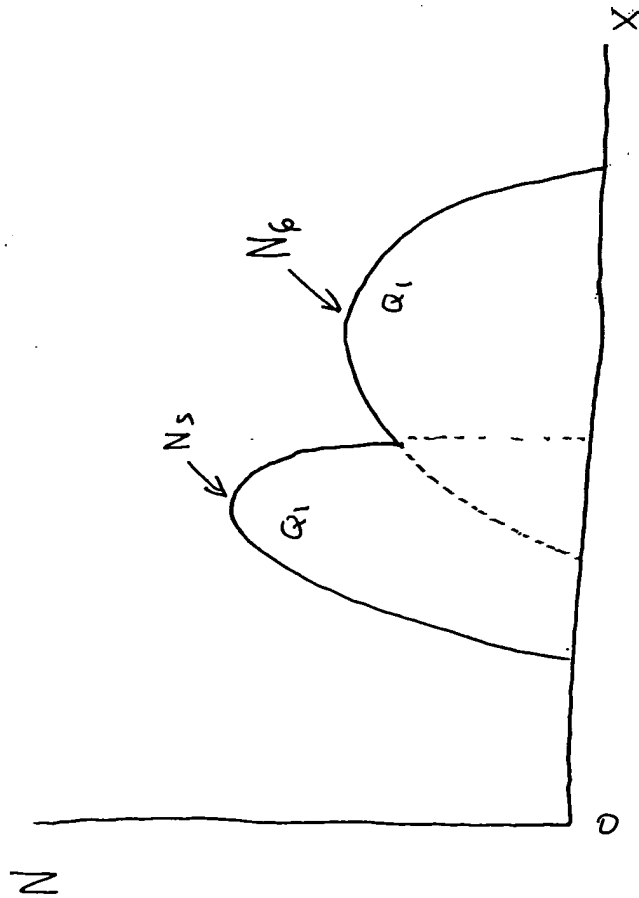


Fig. 17N

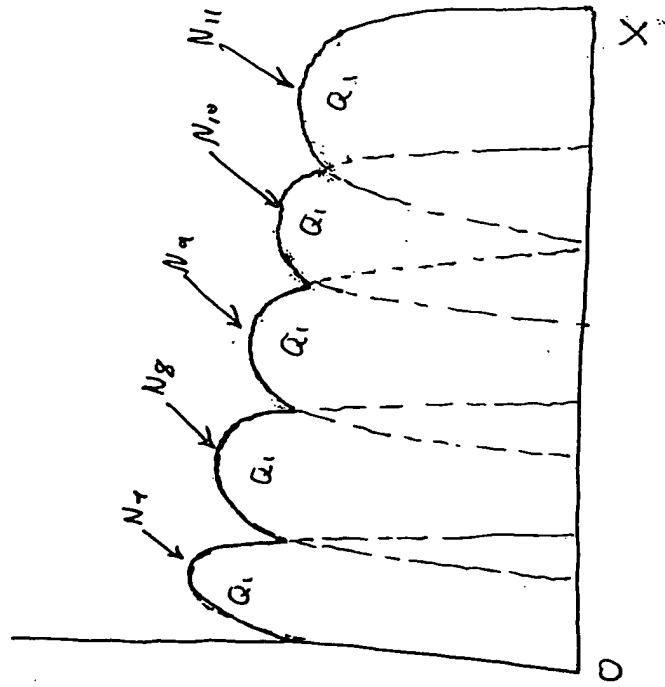


Fig. 17P

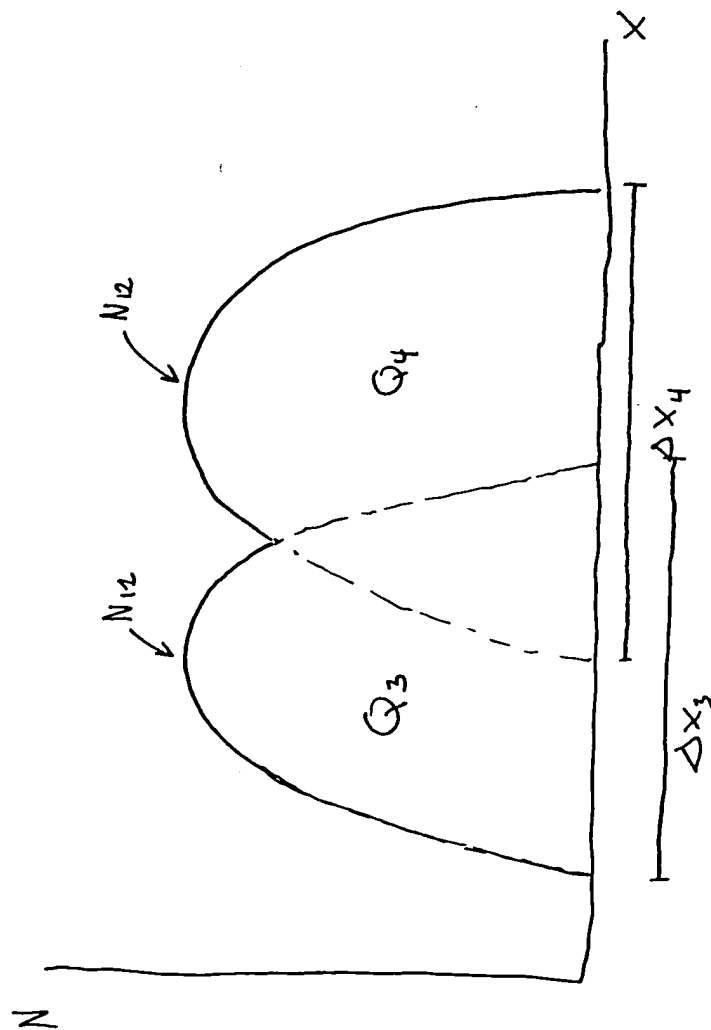


Fig. 17Q

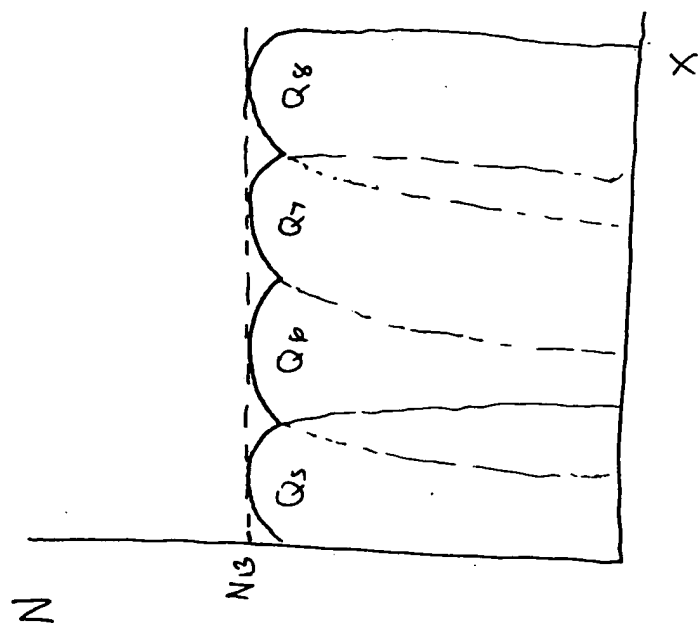


Fig. 17R

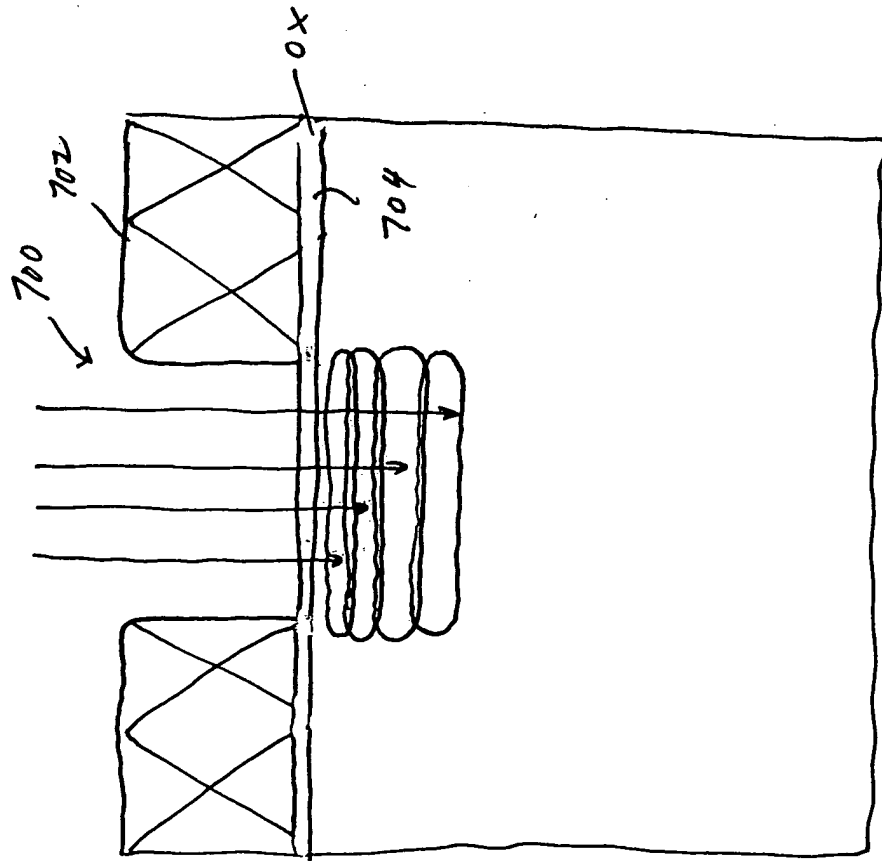


Fig. 17S

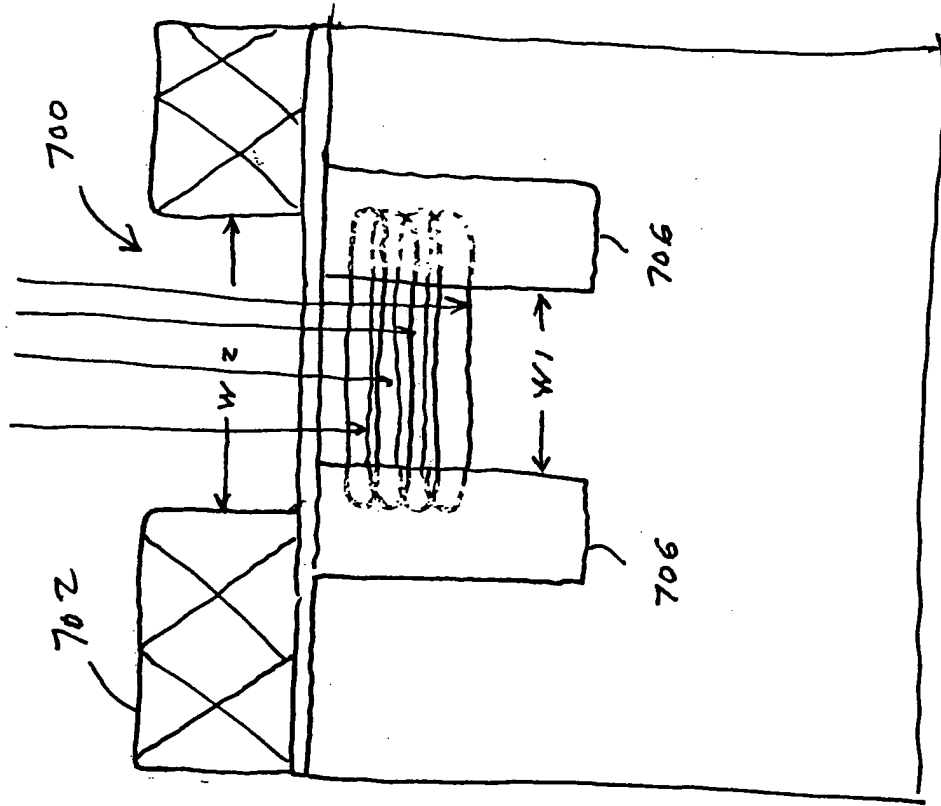


Fig. 17T

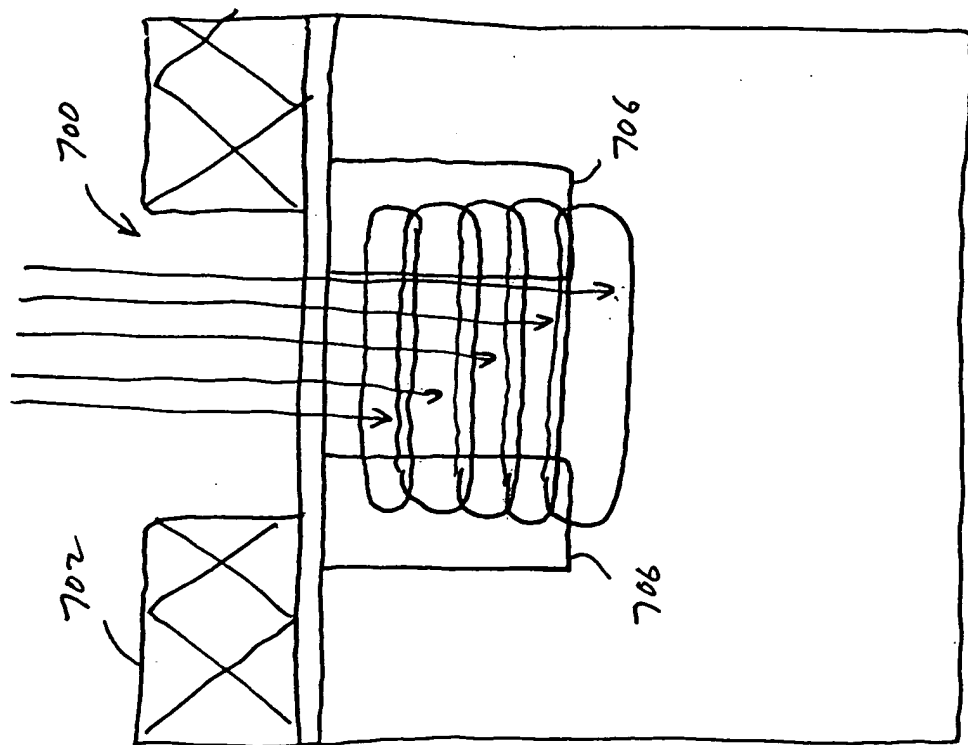
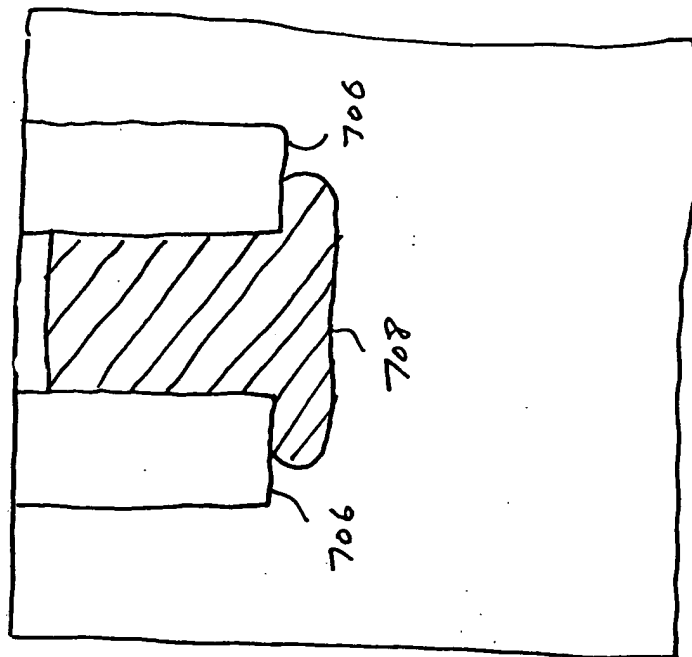


Fig. 17U



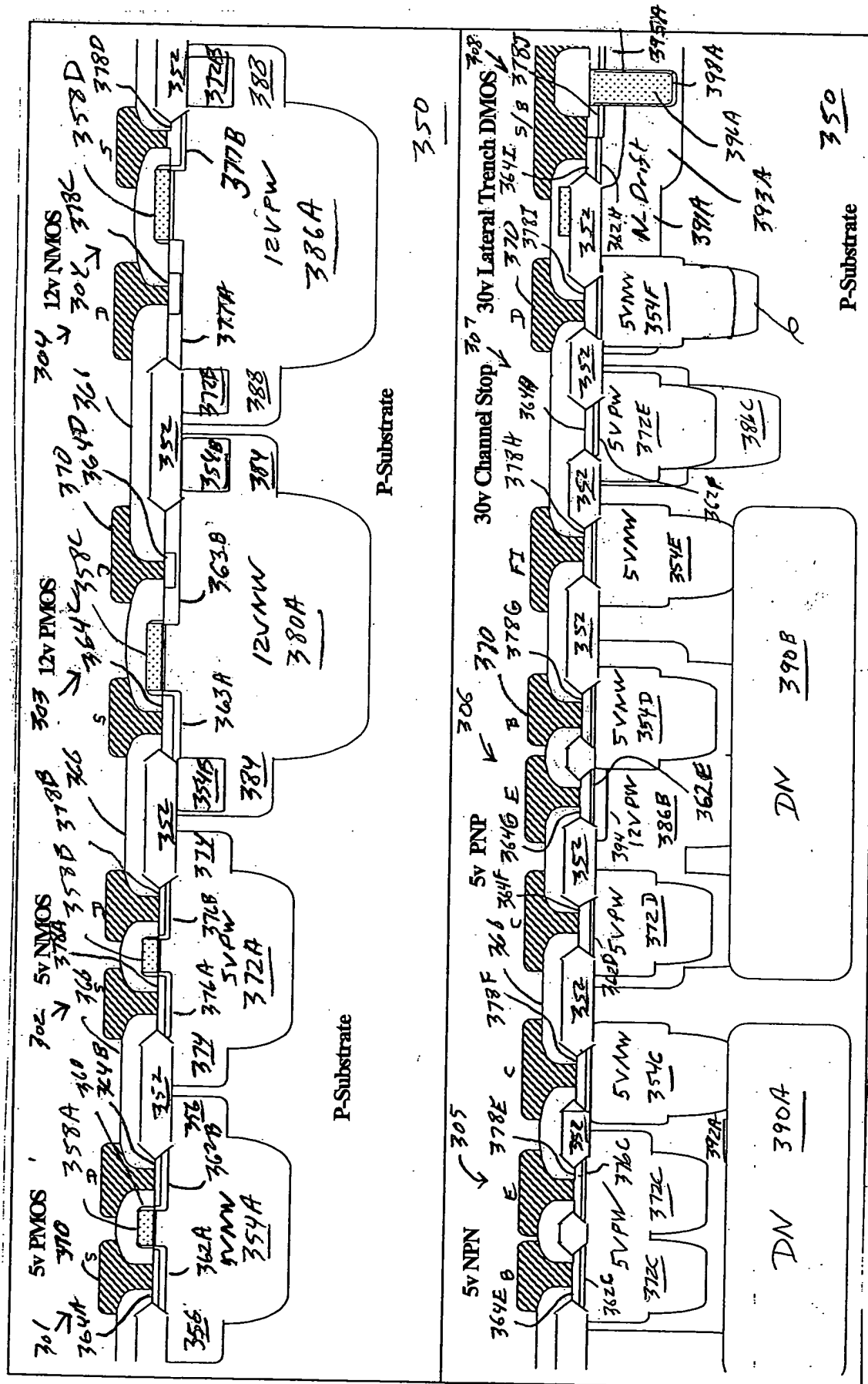


Fig. 18A

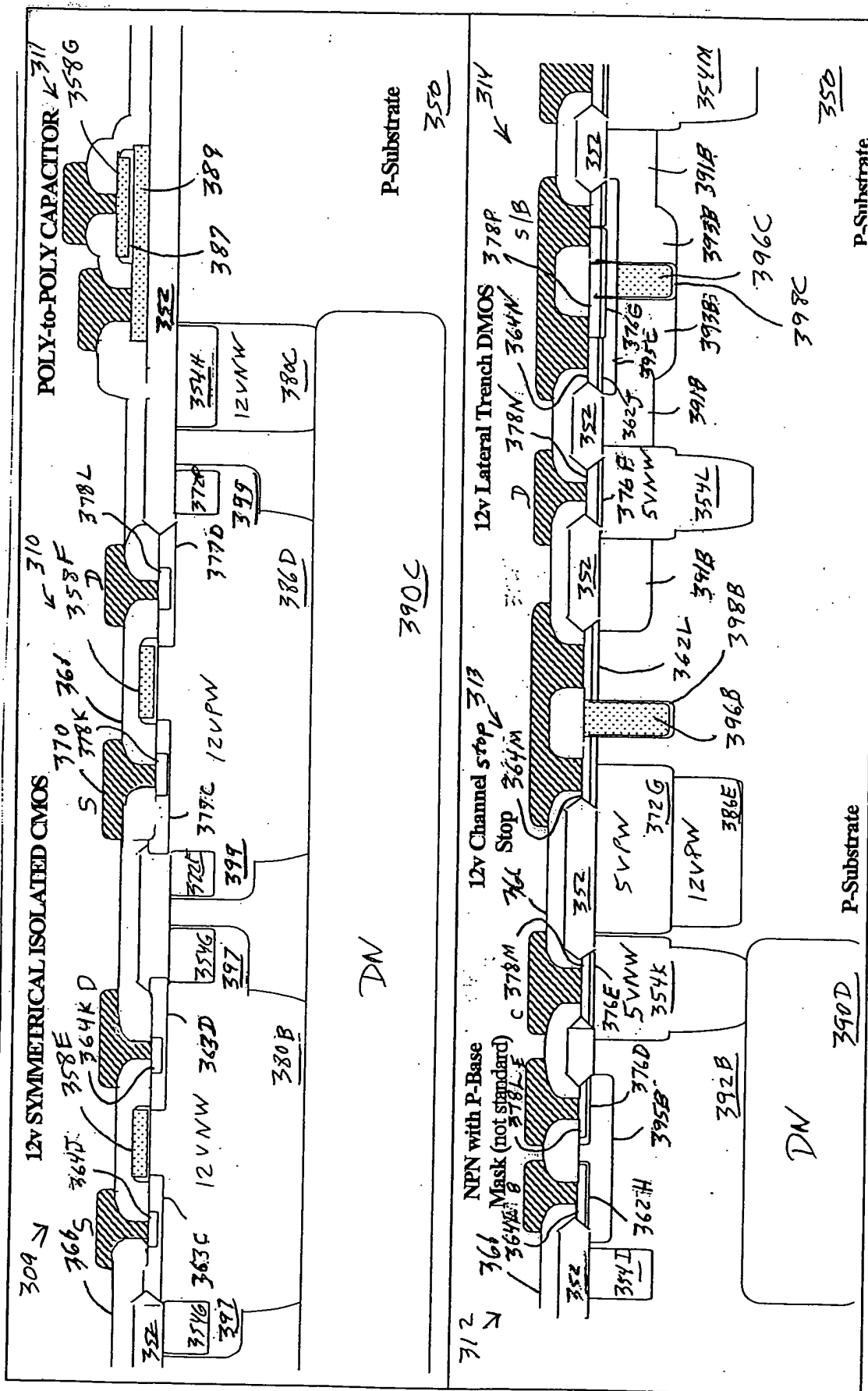
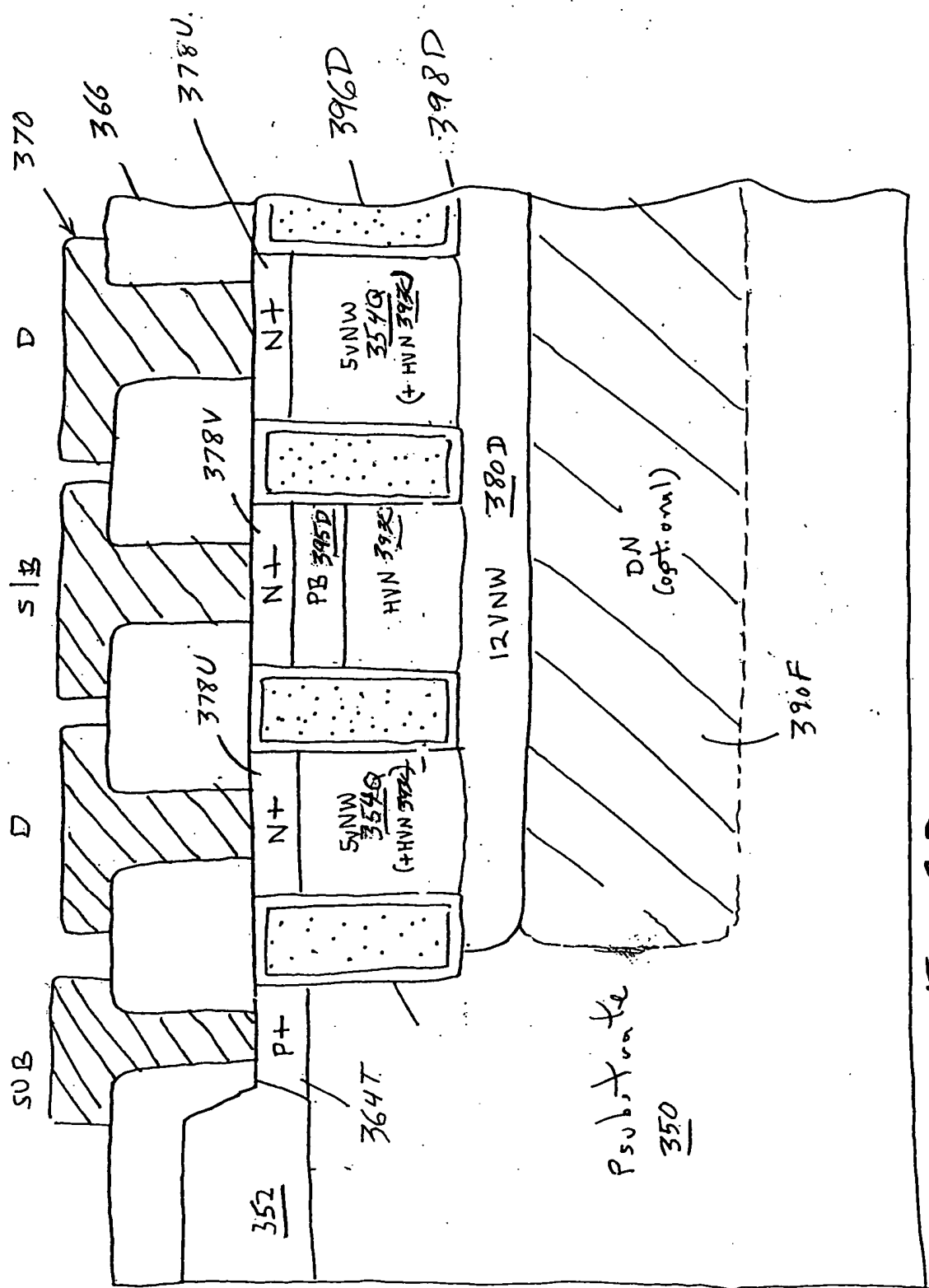


Fig. 18B

300

317

79/219



350
Psub, Tsub, Tsub

318

300

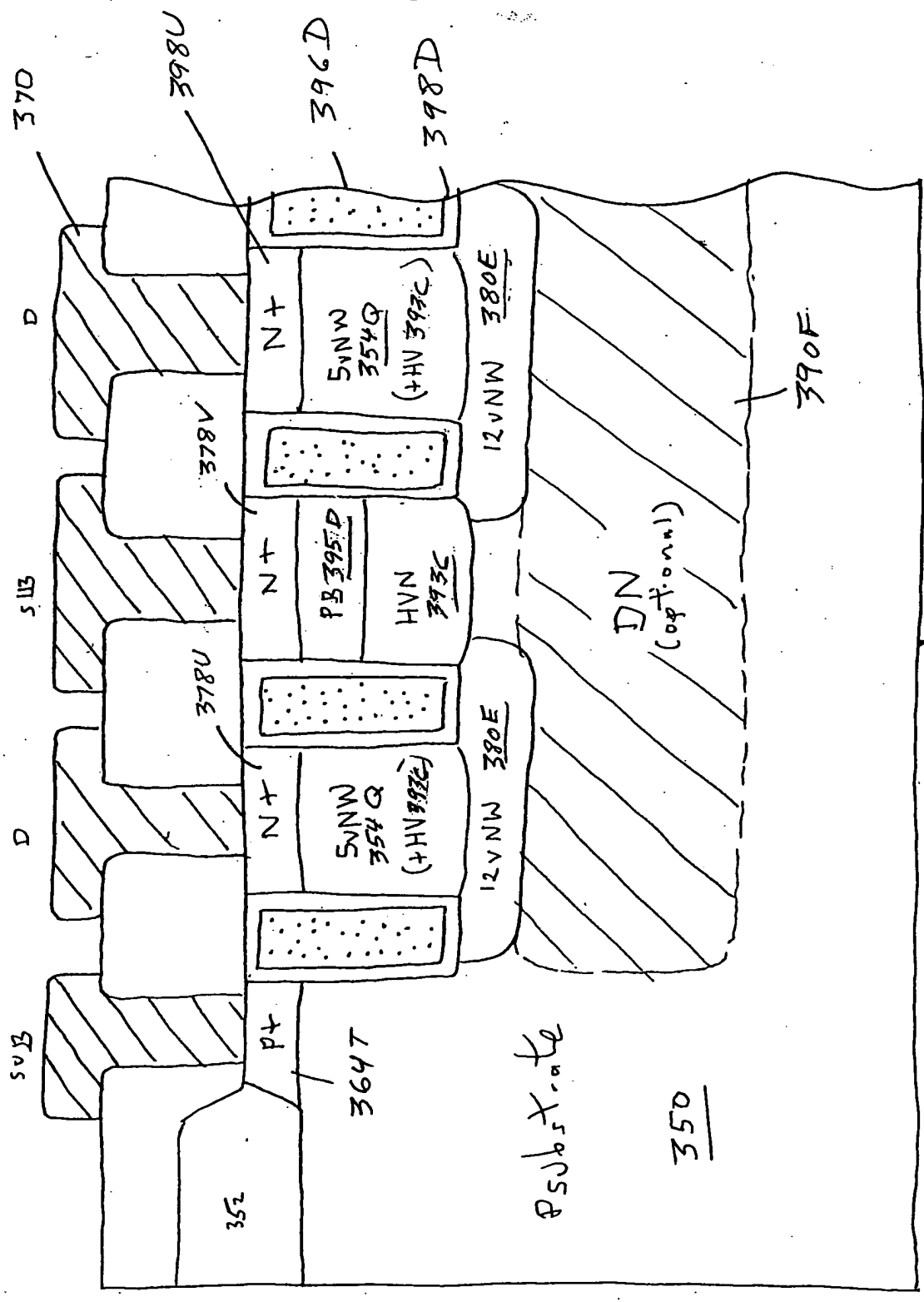
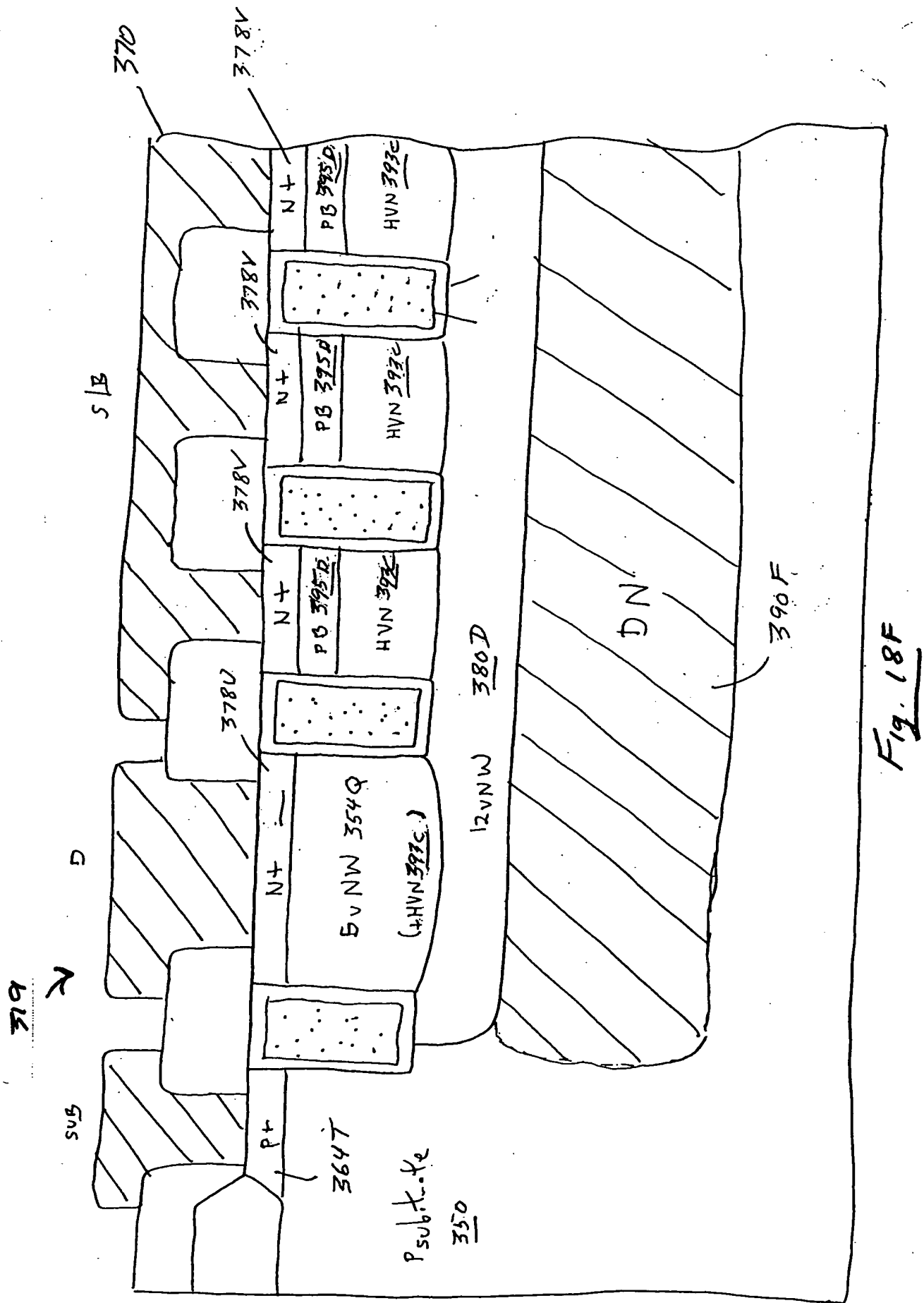


Fig. 18E



82/219

Q23

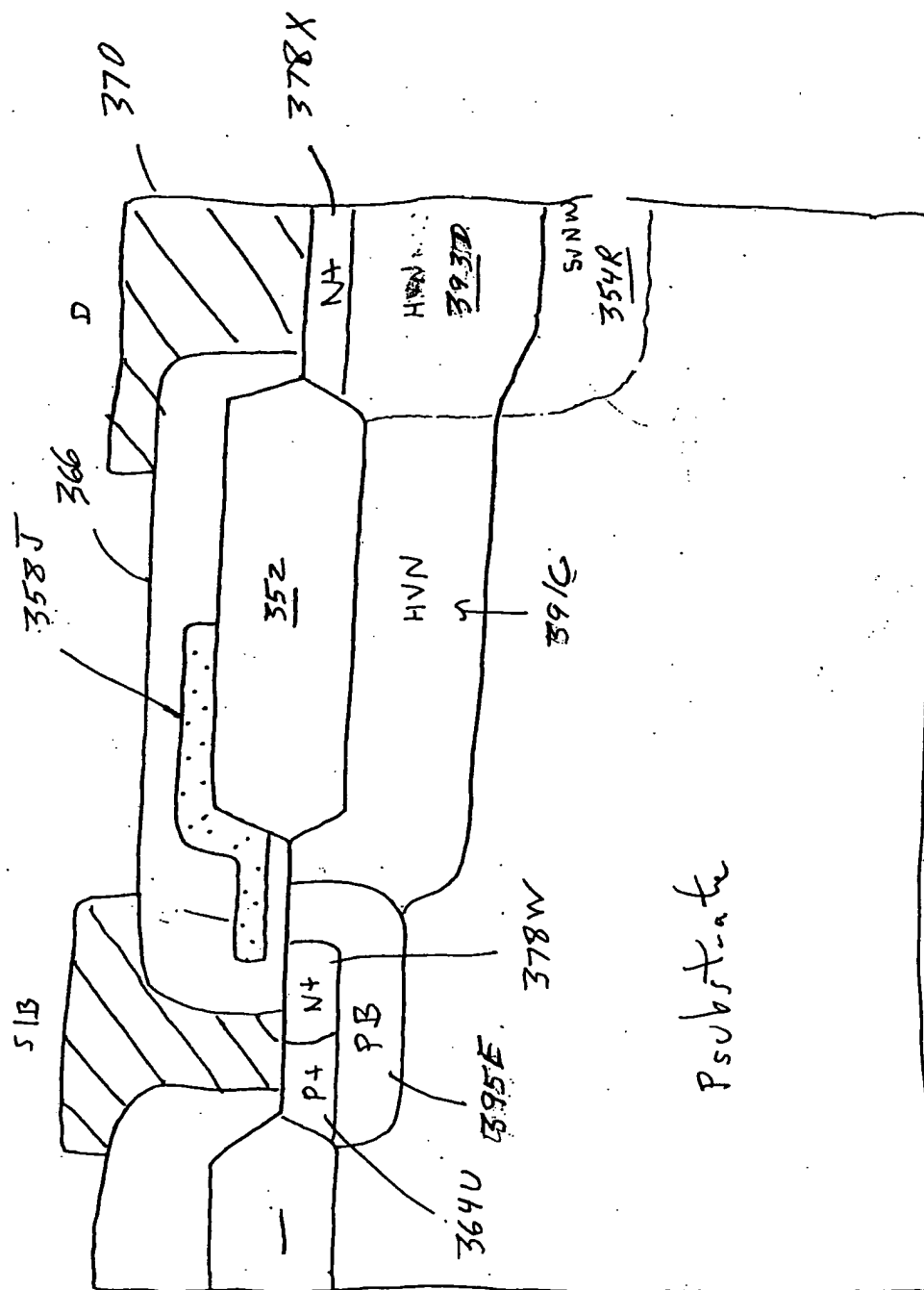
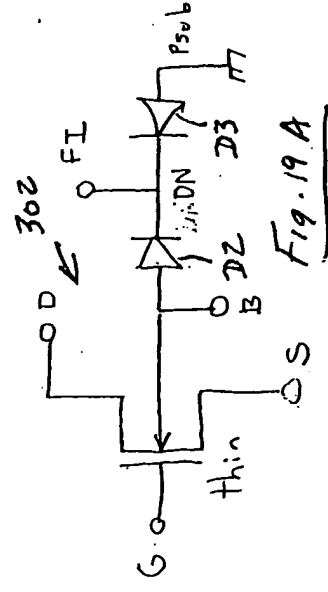
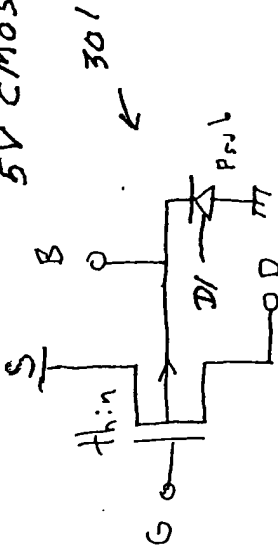


Fig 186

5V CMOS



5V NPN

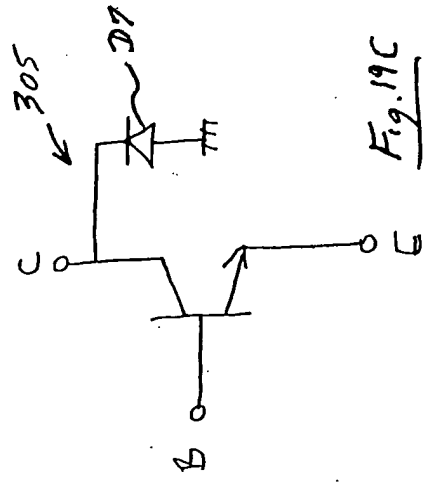


Fig. 19C

12V CMOS

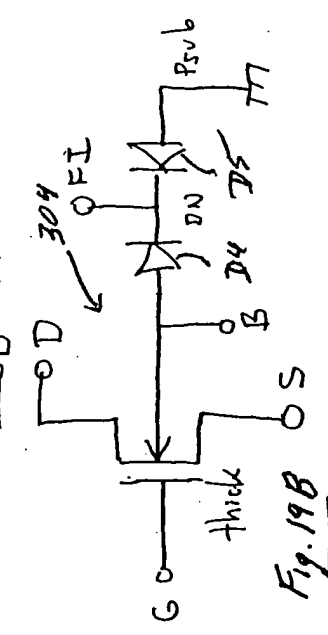
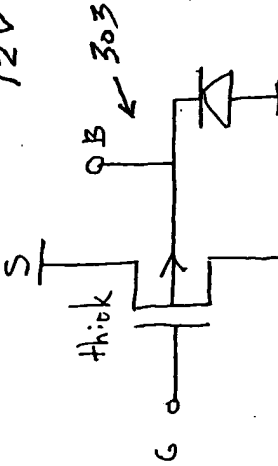


Fig. 19B

5V PNP

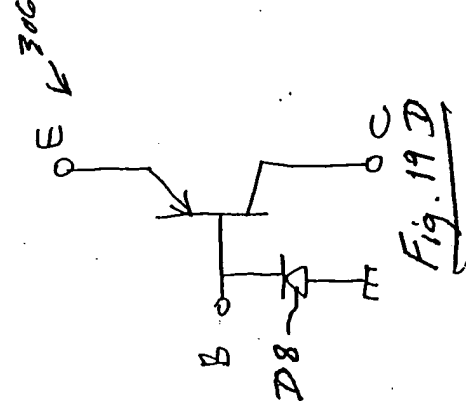


Fig. 19D

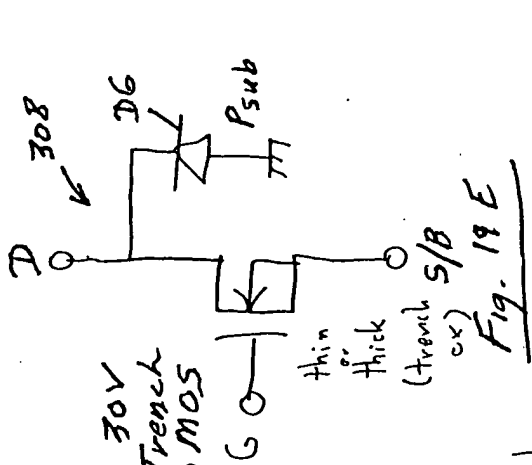


Fig. 19E

30V LDMOS

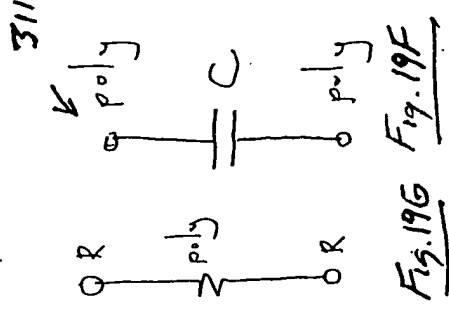


Fig. 19F

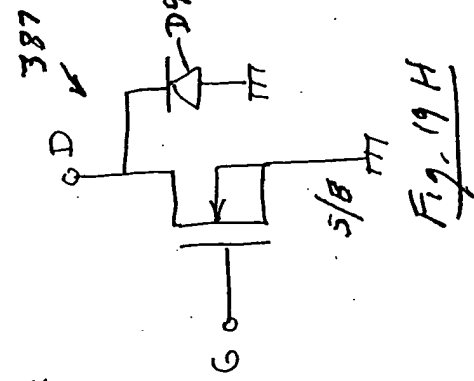
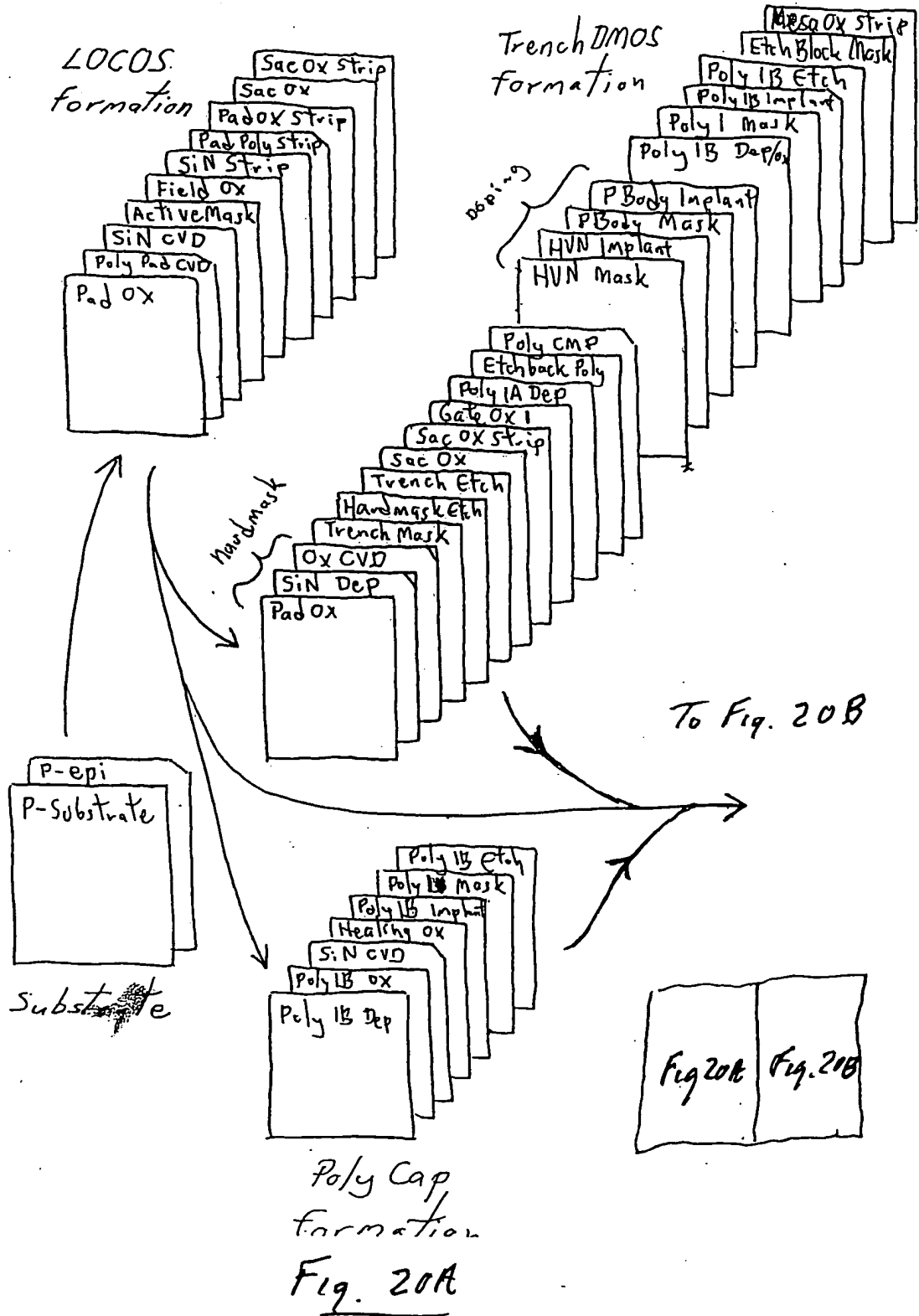


Fig. 19H

84/219



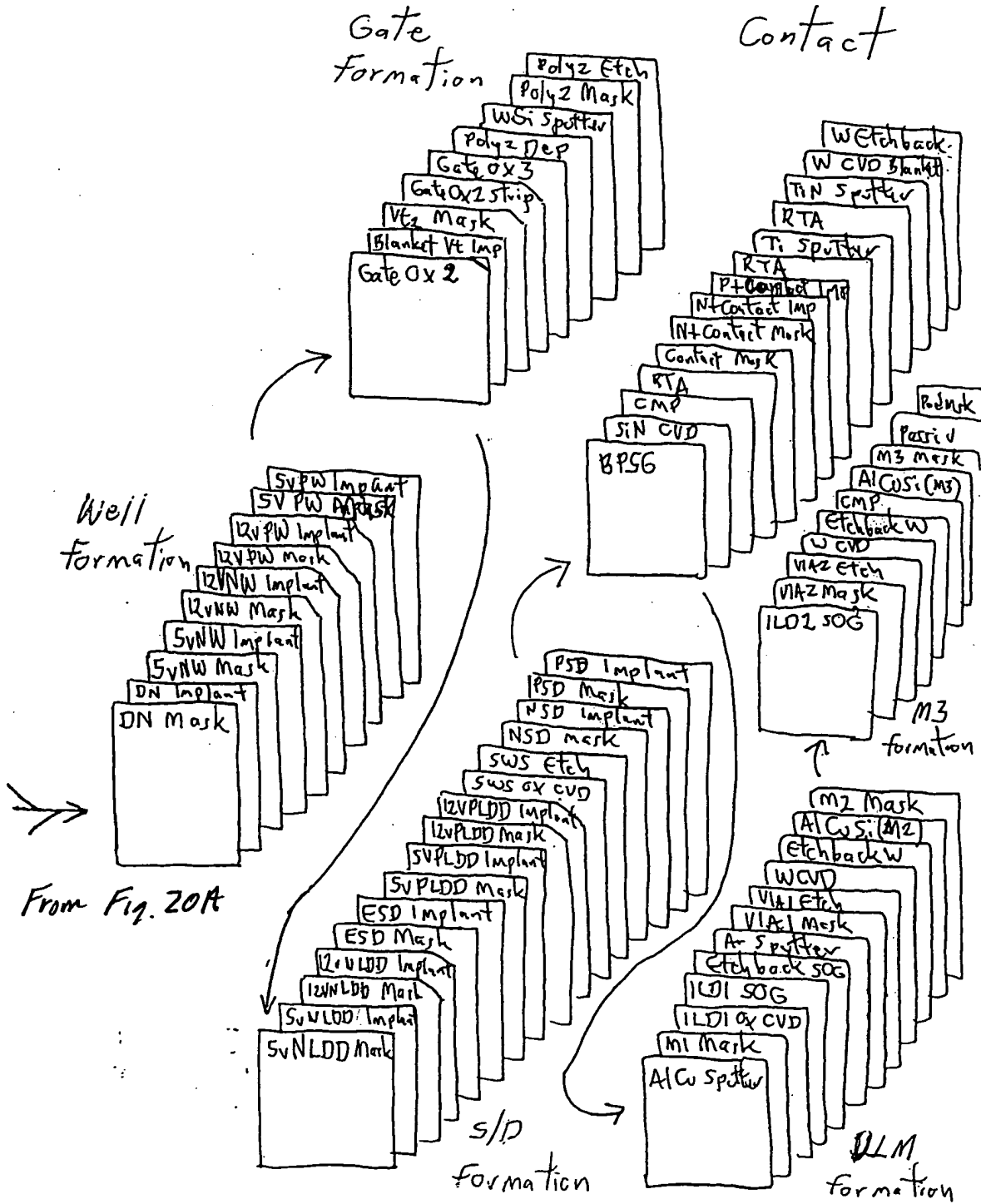
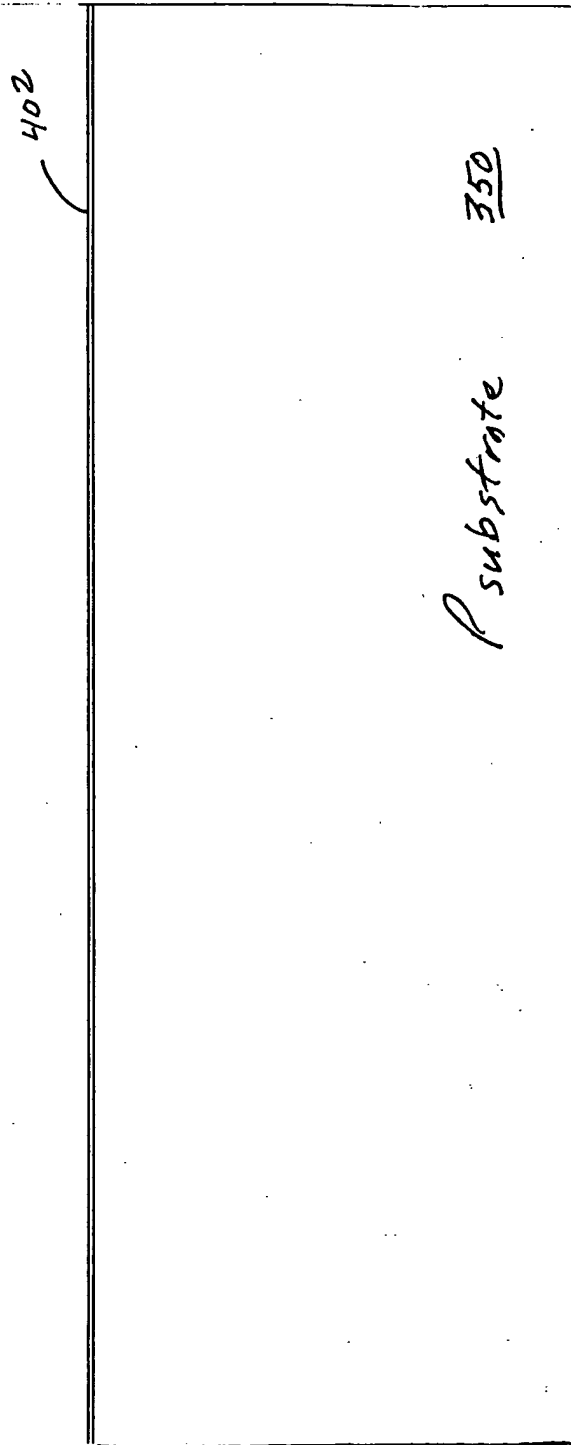


Fig. 20B

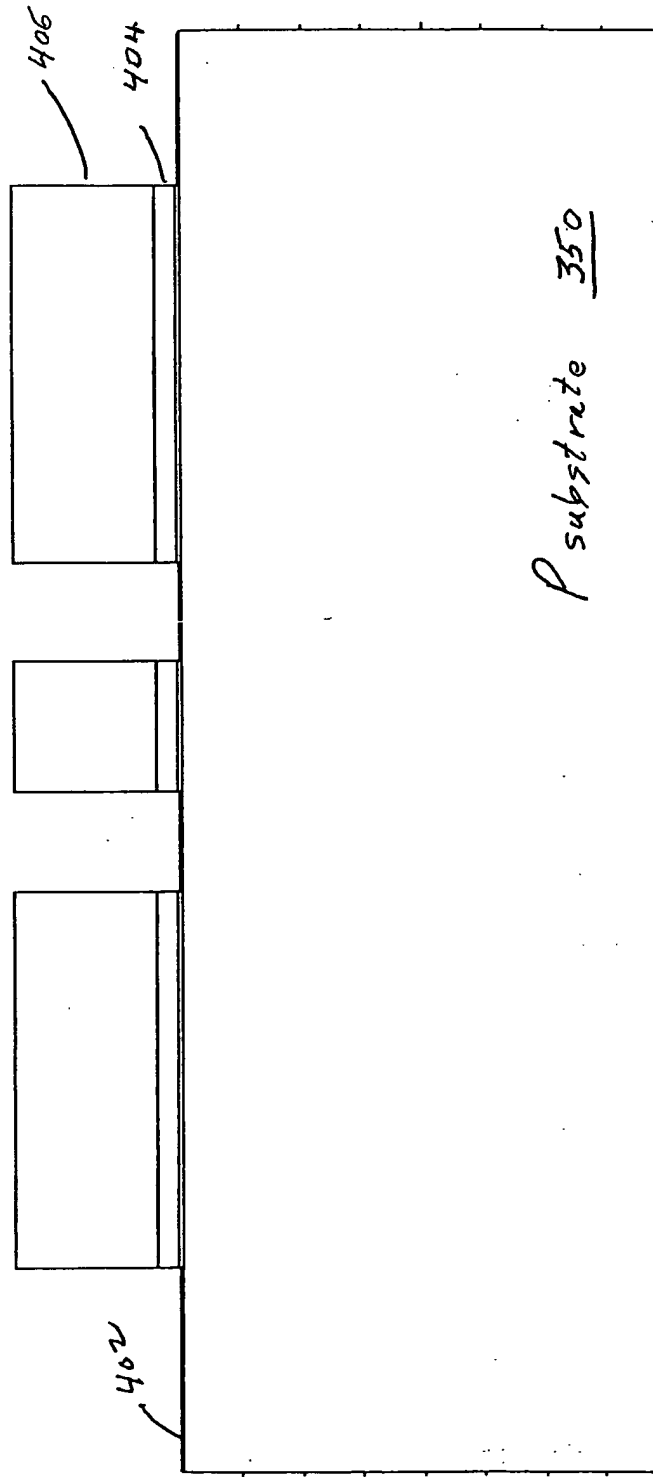


First Pad Oxide Layer

Fig. 21

5V PMOS 301

5V NMOS 302

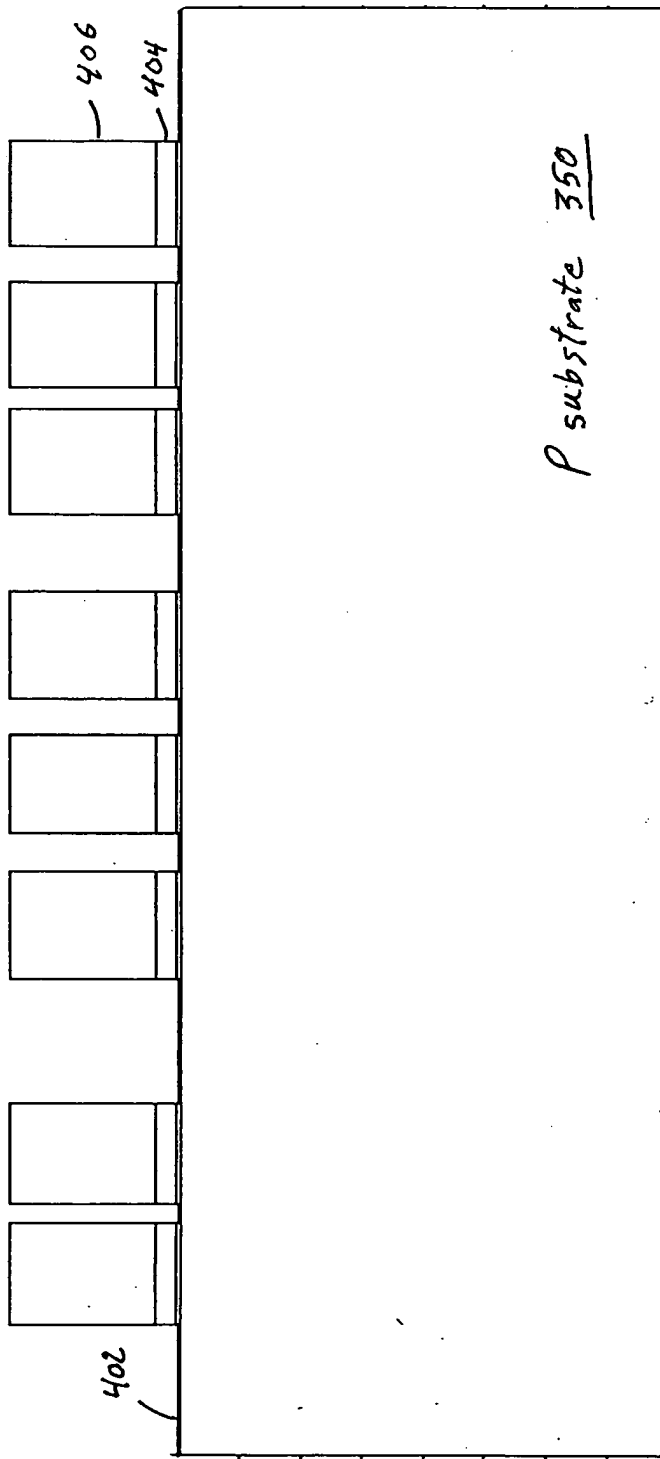


LOCOS - Nitride Mask and Etch

Fig. 22A

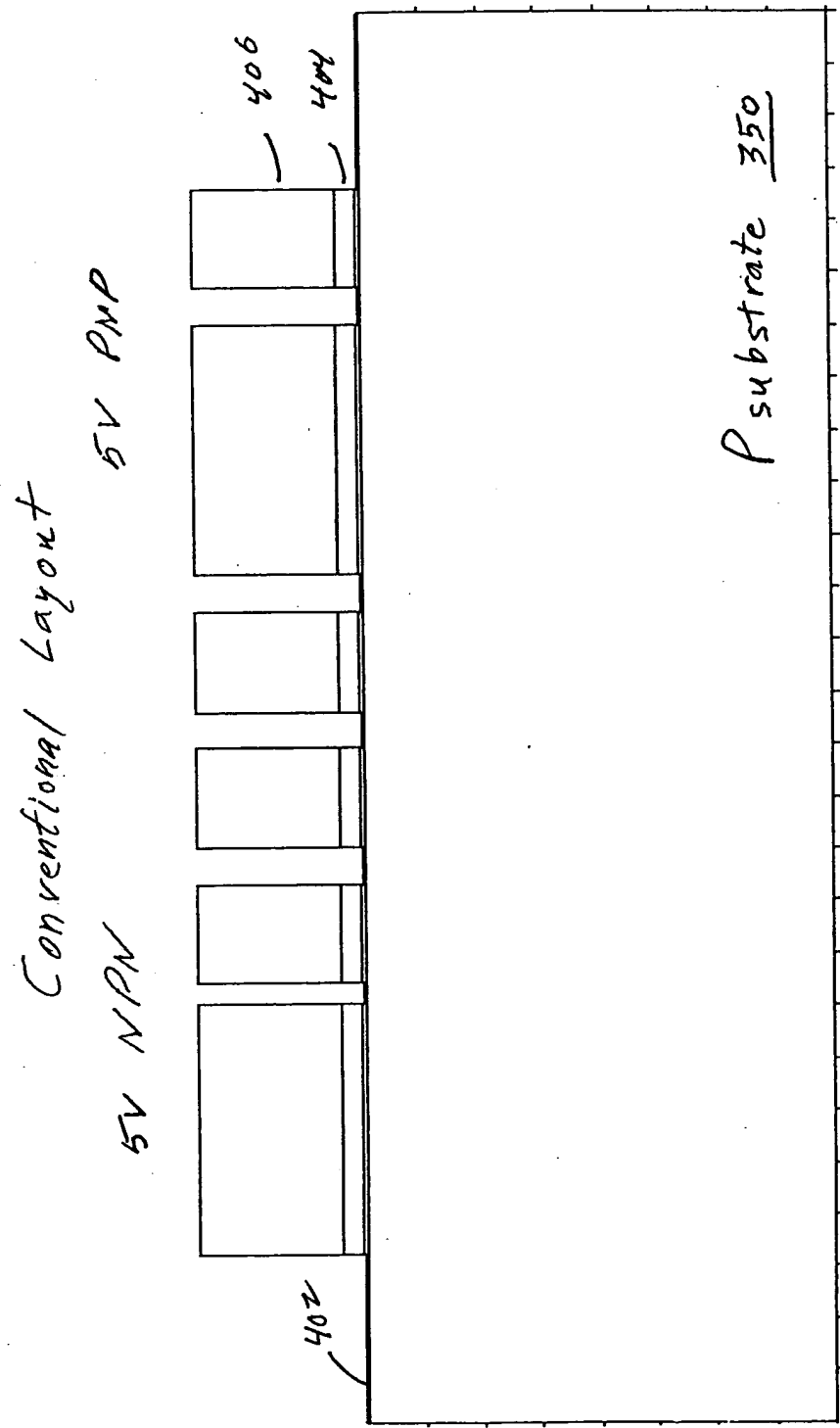
87/219

High F_T Layout
5V NPN 305 5V PNP 306



Locos - Nitride Mask and Etch

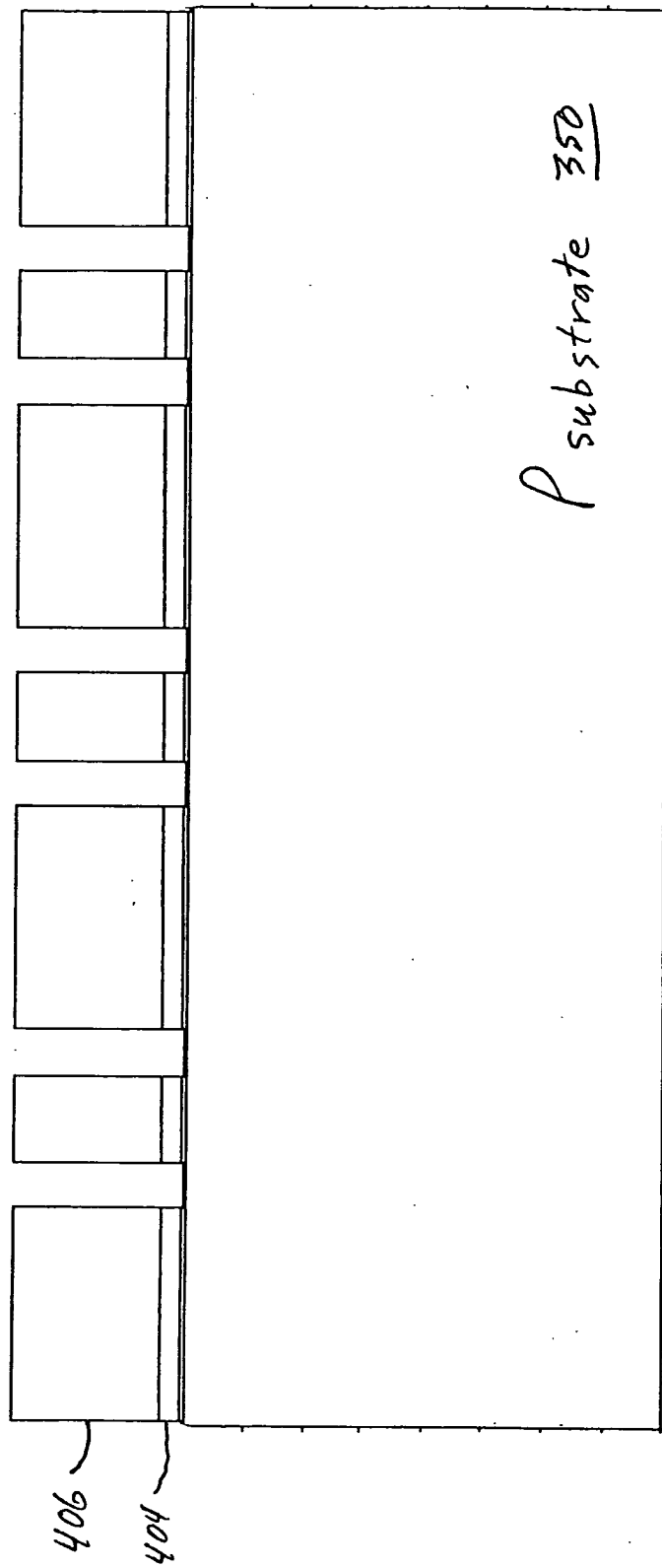
Fig. 22B



LOCOS - Nitride Mask and Etch

Fig. 22C

30V Lateral Trench DMOS 308



LOCOS - Nitride Mask and Etch

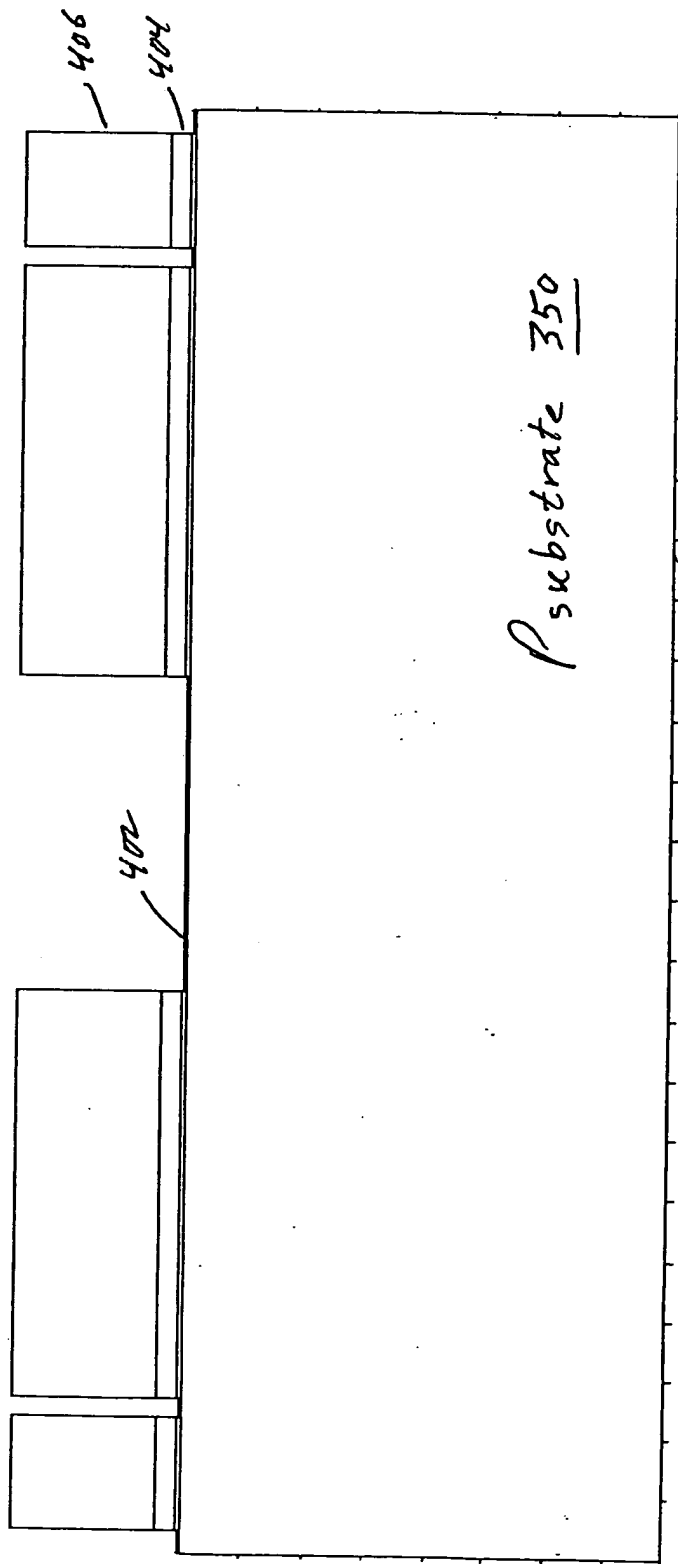
Fig. 22D

90/219

Symmetrical 12V CMOS

12V PMOS 309

12V NMOS 310

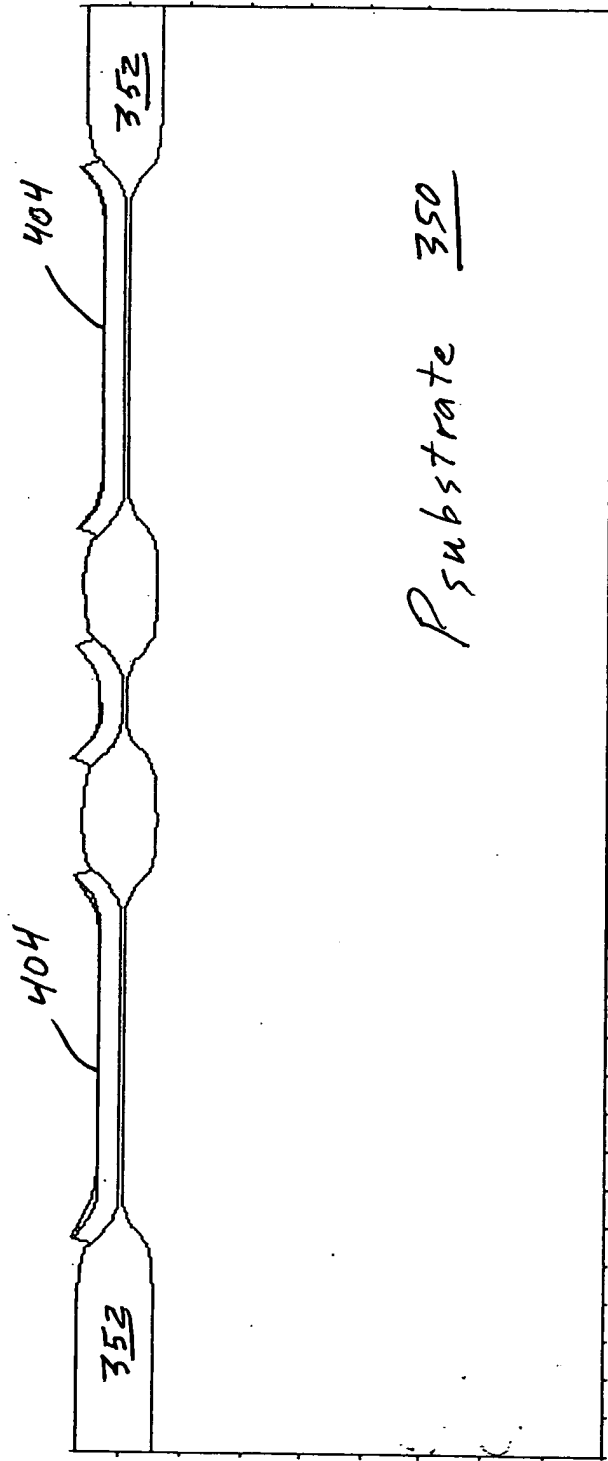


LOCOS - Nitride Mask and Etch

Fig. 22E

5V PMOS 301

5V NMOS 302

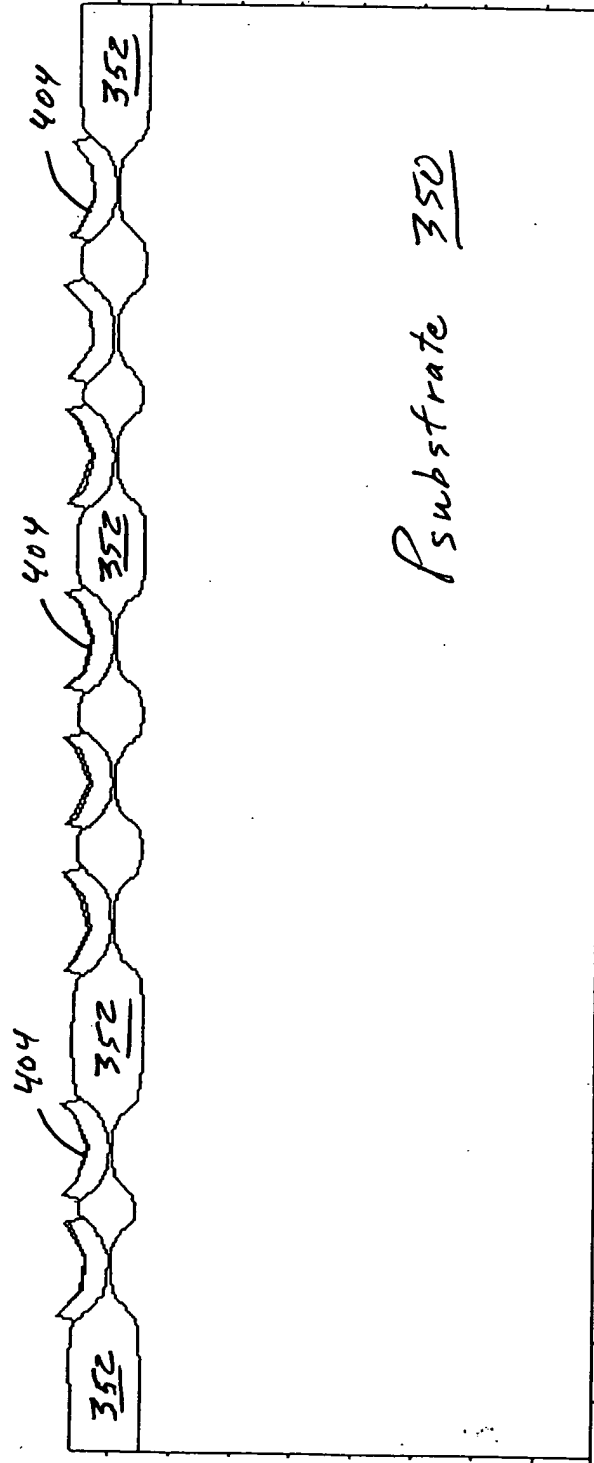


LOCOS - Field Oxidation
Fig. 23A

High F_T Layout

5V NPN 305

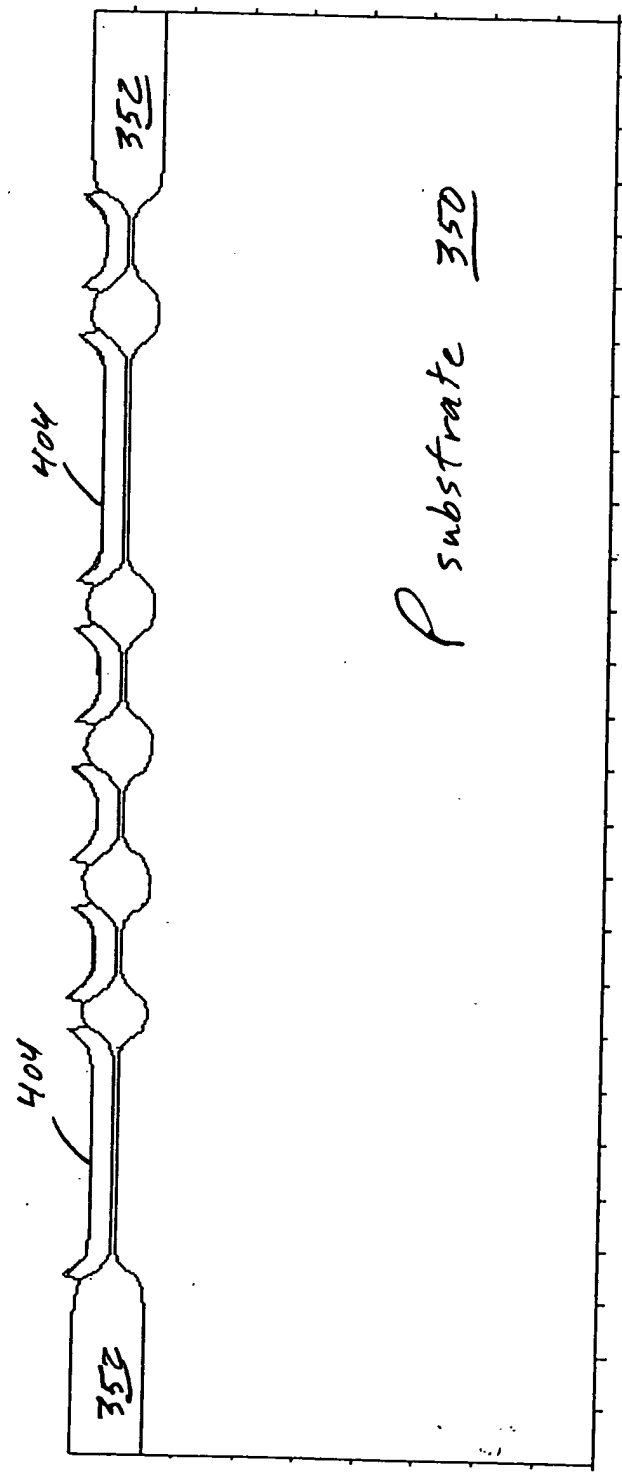
5V PNP 306



20005 - Field Oxidation

Fig. 23B

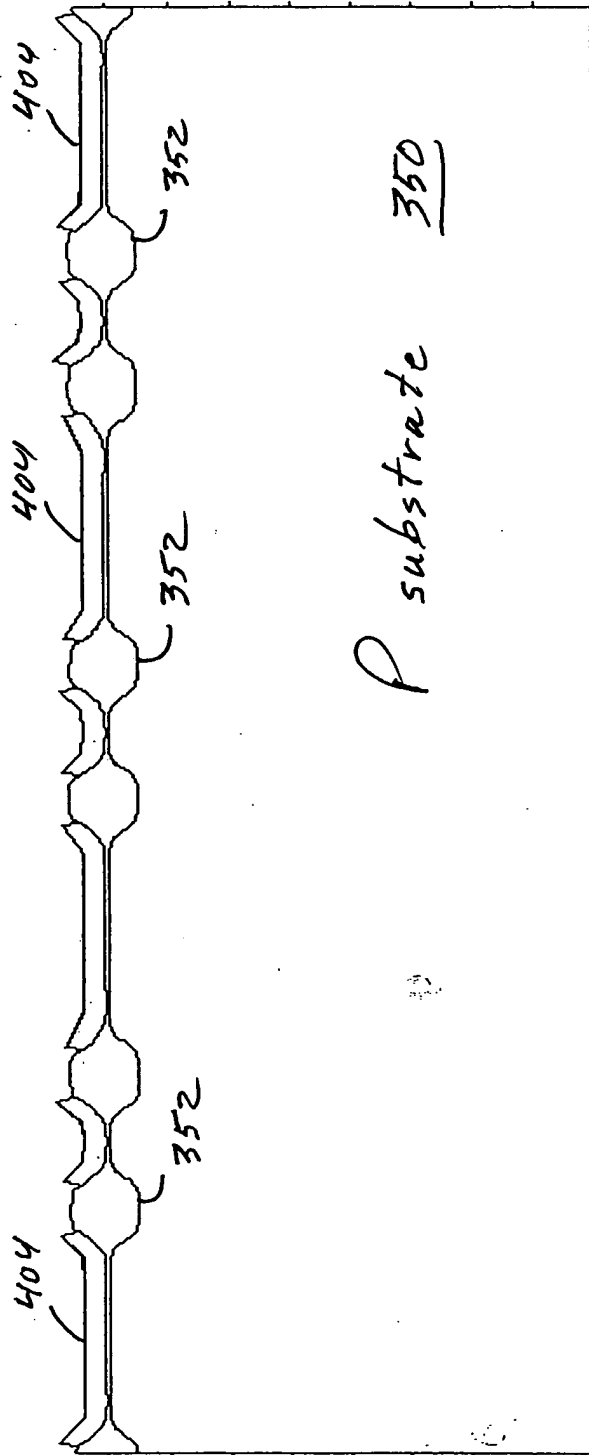
Conventional Layout
5V NPN 5V PNP



LOCOS-Field Oxidation

Fig 23C

30V Lateral Trench DMOS



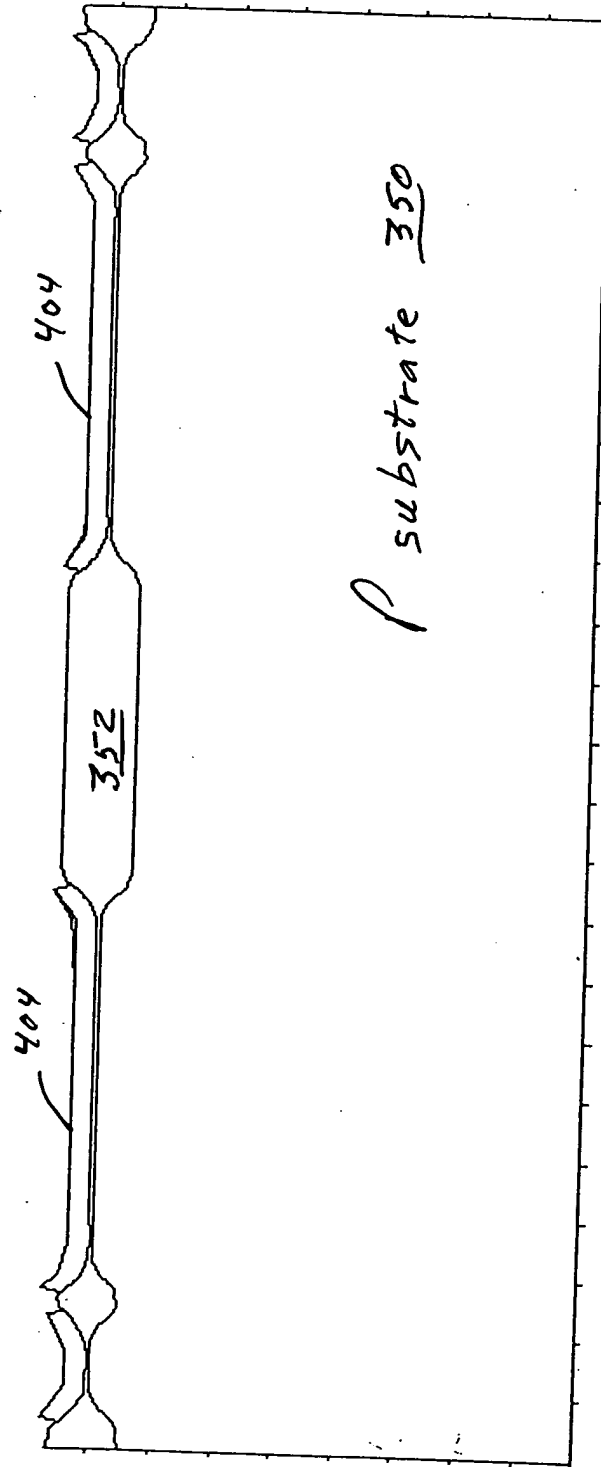
LOCOS - Field Oxidation

Fig. 23D

96/219

Symmetrical 12V CMOS

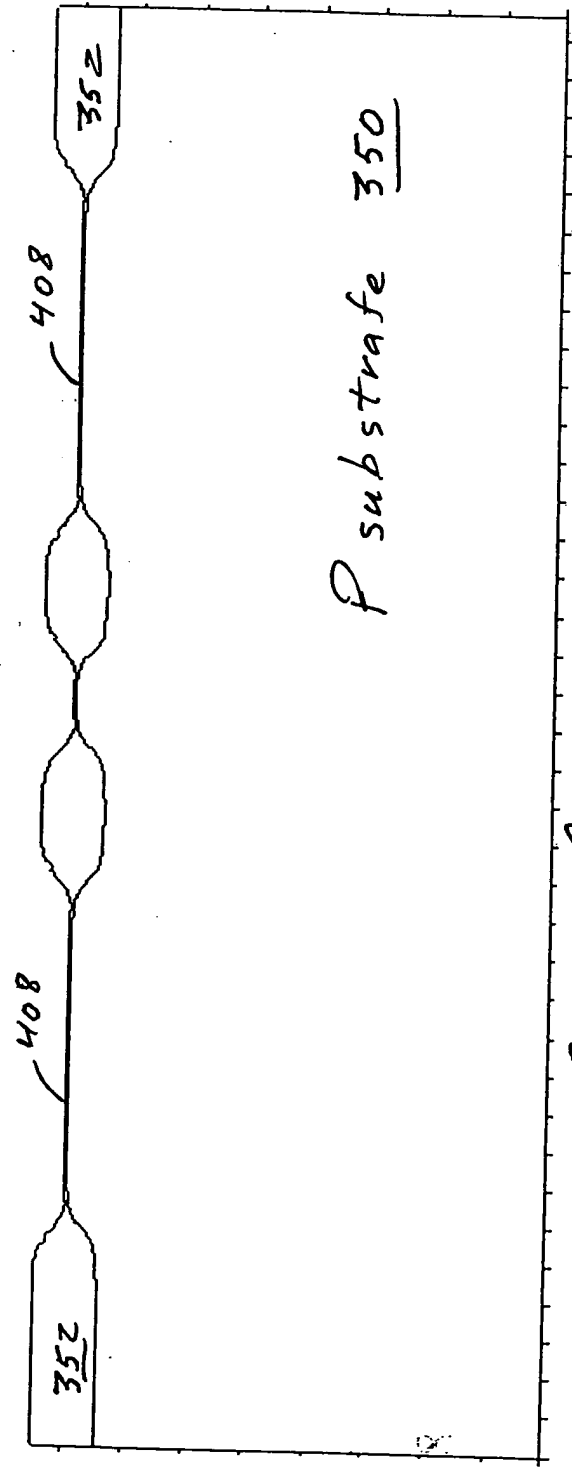
12V PMOS 309 12V NMOS 310



LOCOS - Field Oxidation

Fig. 23E

5V PMOS 301 5V NMOS 302



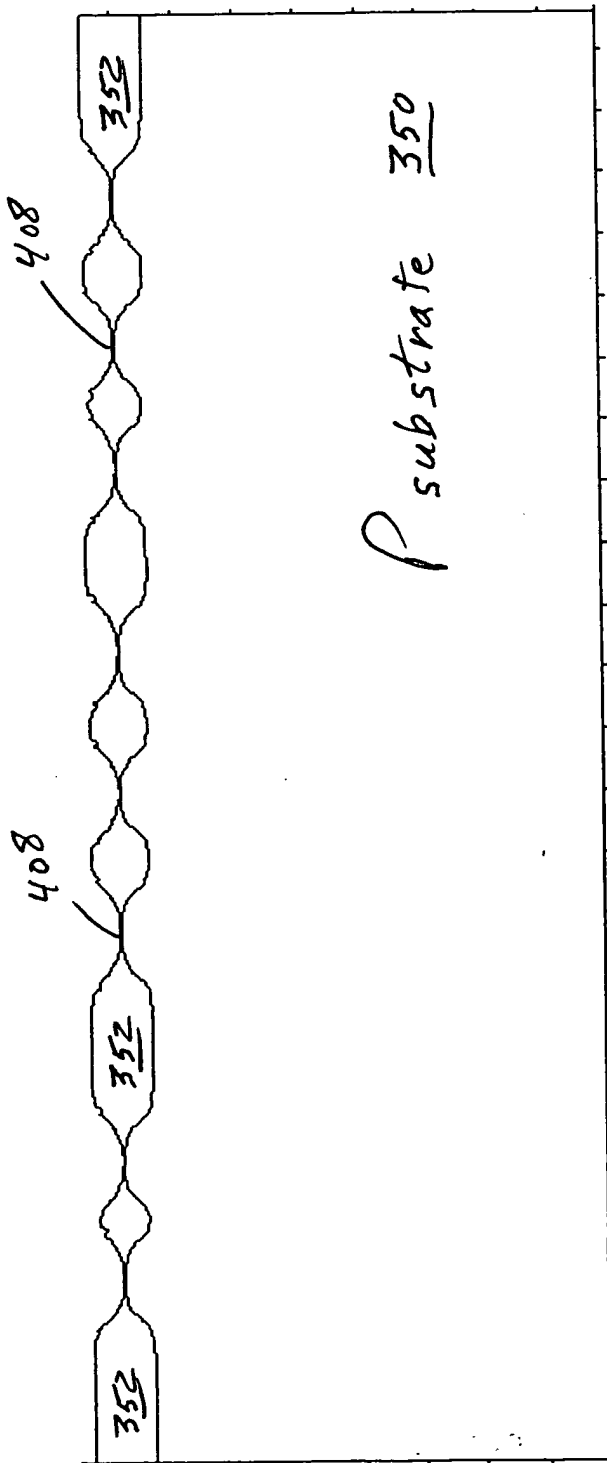
Second Pad Oxide Layer

Fig. 24A

High F_T Layout

5V NPN 305

5V PNP 306



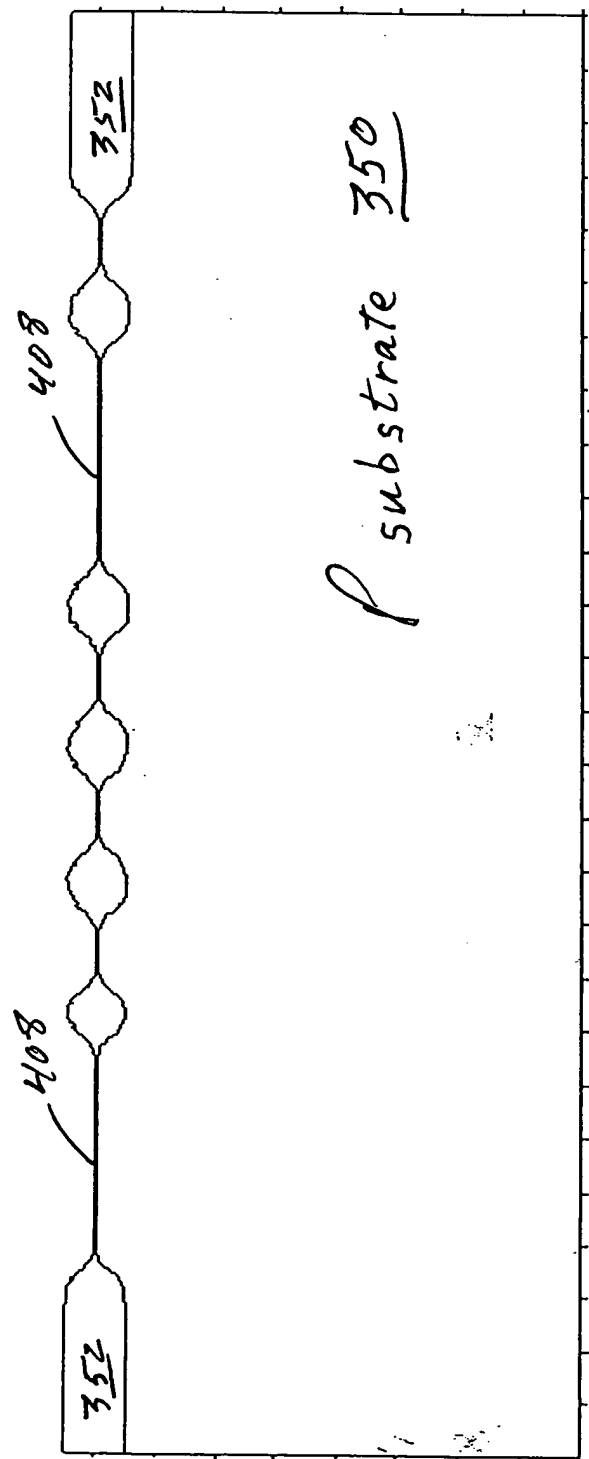
Second Pad Oxide Layer

Fig. 24B

98/219

Conventional layout

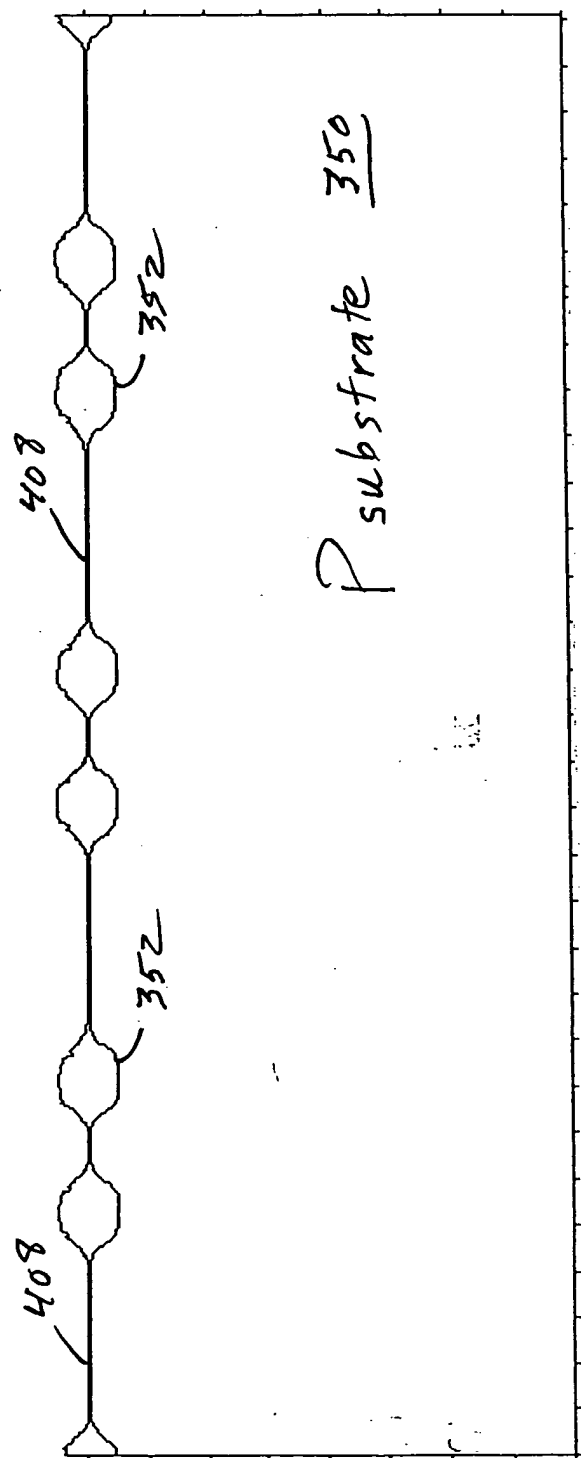
5V NPN 5V PNP



Second Pad Oxide Layer

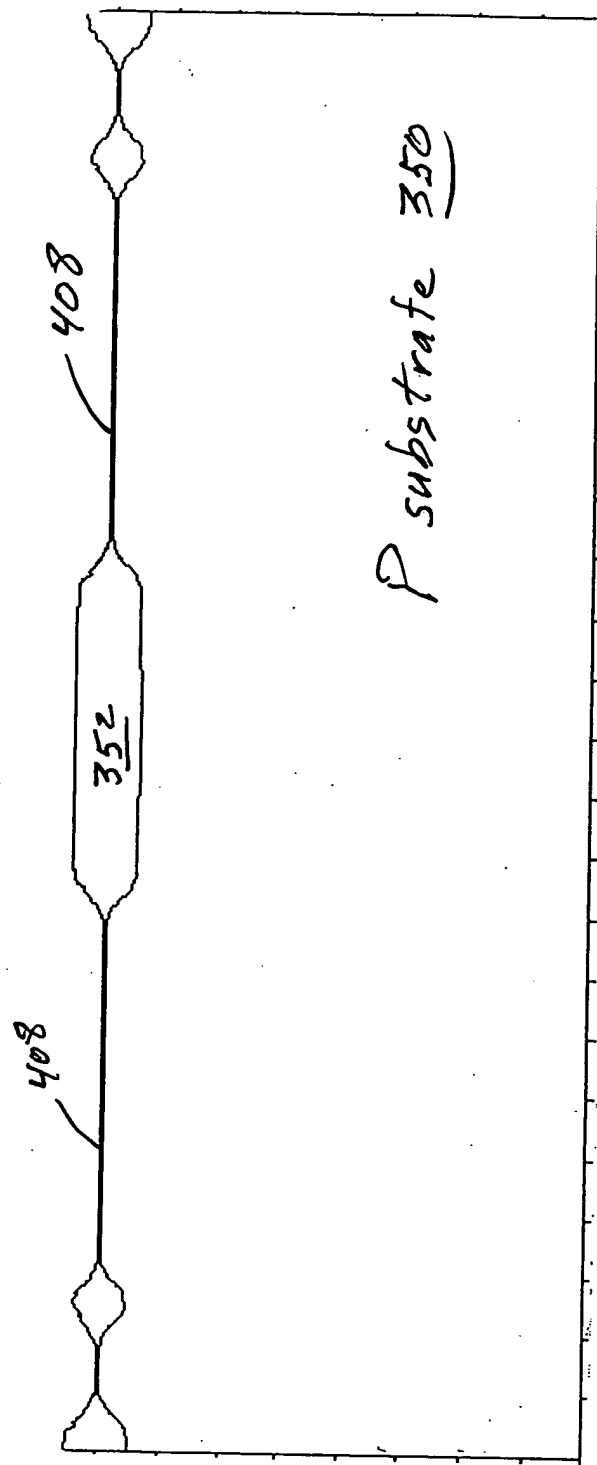
Fig. 24C

30V Lateral Trench DMOS 308



Second Pad Oxide Layer
Fig 24D

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



Second Pad Oxide Layer
 Fig. 24E

102/219

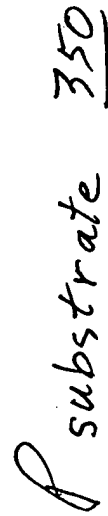
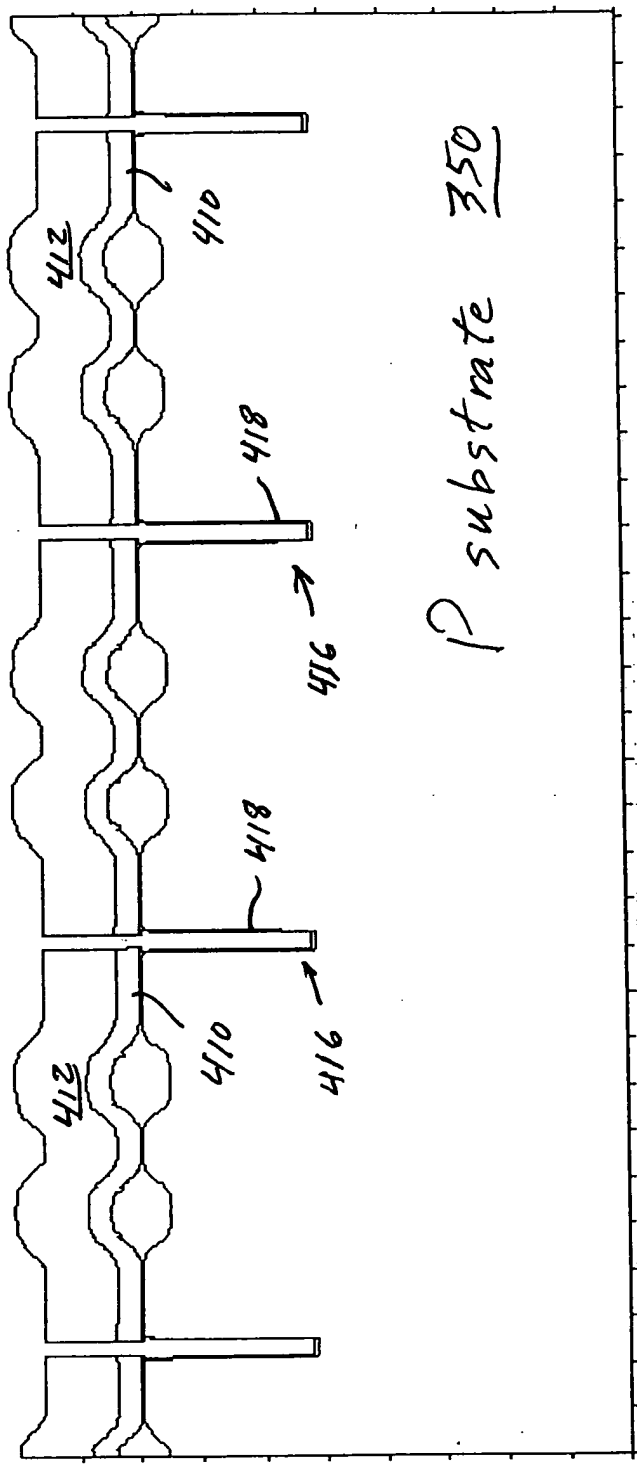


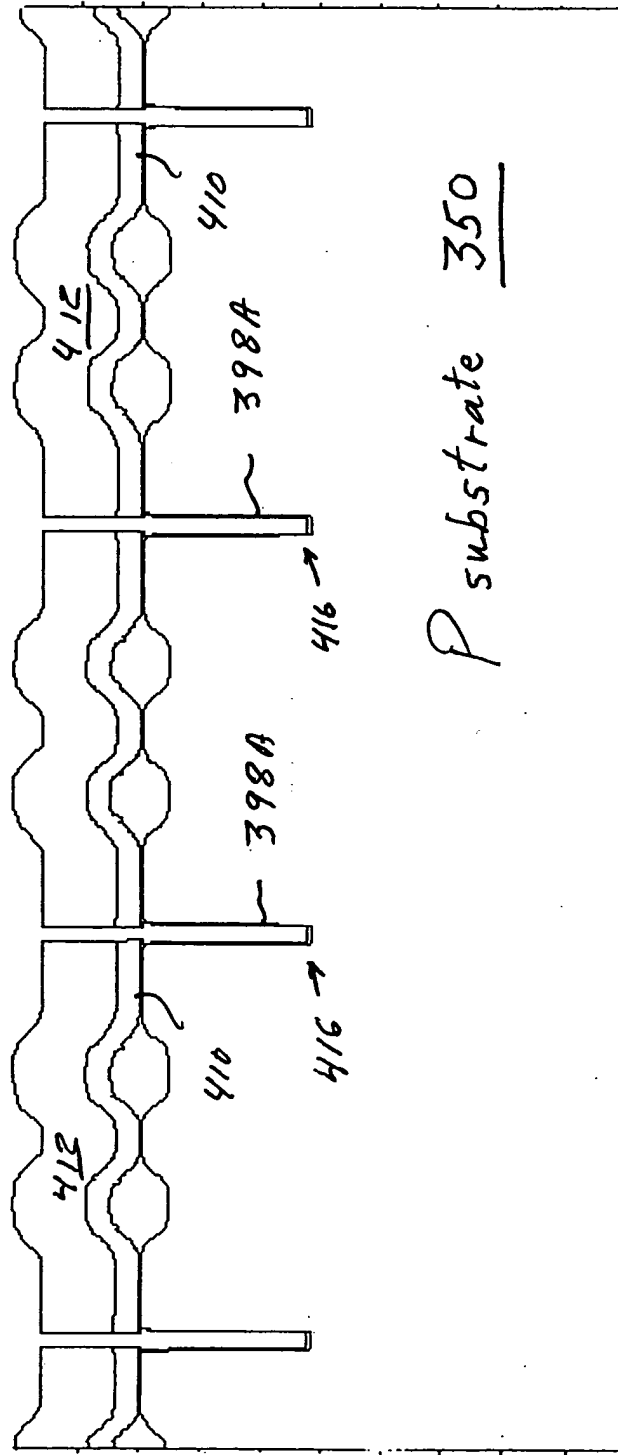
Fig. 25-D

30V Lateral Trench DMOS 308



Sacrificial Oxide
Fig. 26D

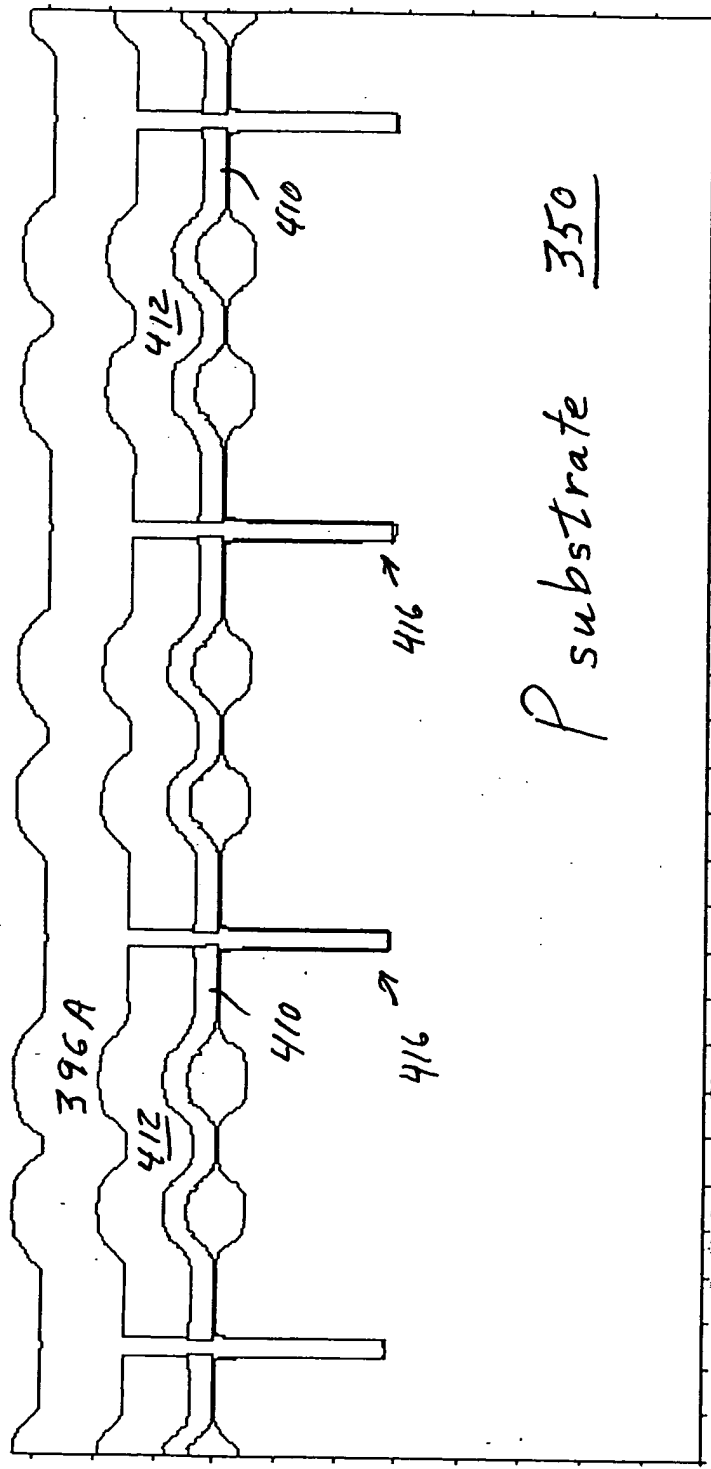
30 V Lateral Trench DMOS 308



Trench Gate Oxide

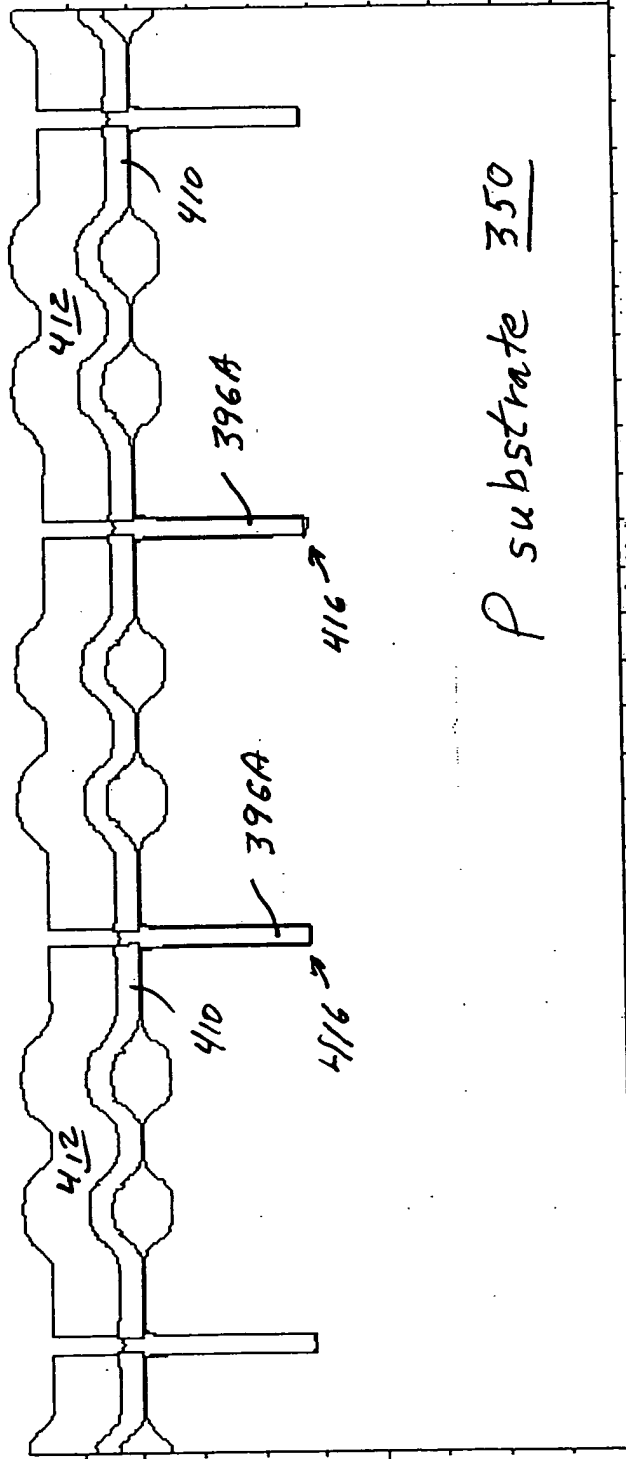
Fig. 27D

30V Lateral Trench DMOS 308



Polysilicon - First Layer
Fig 28D

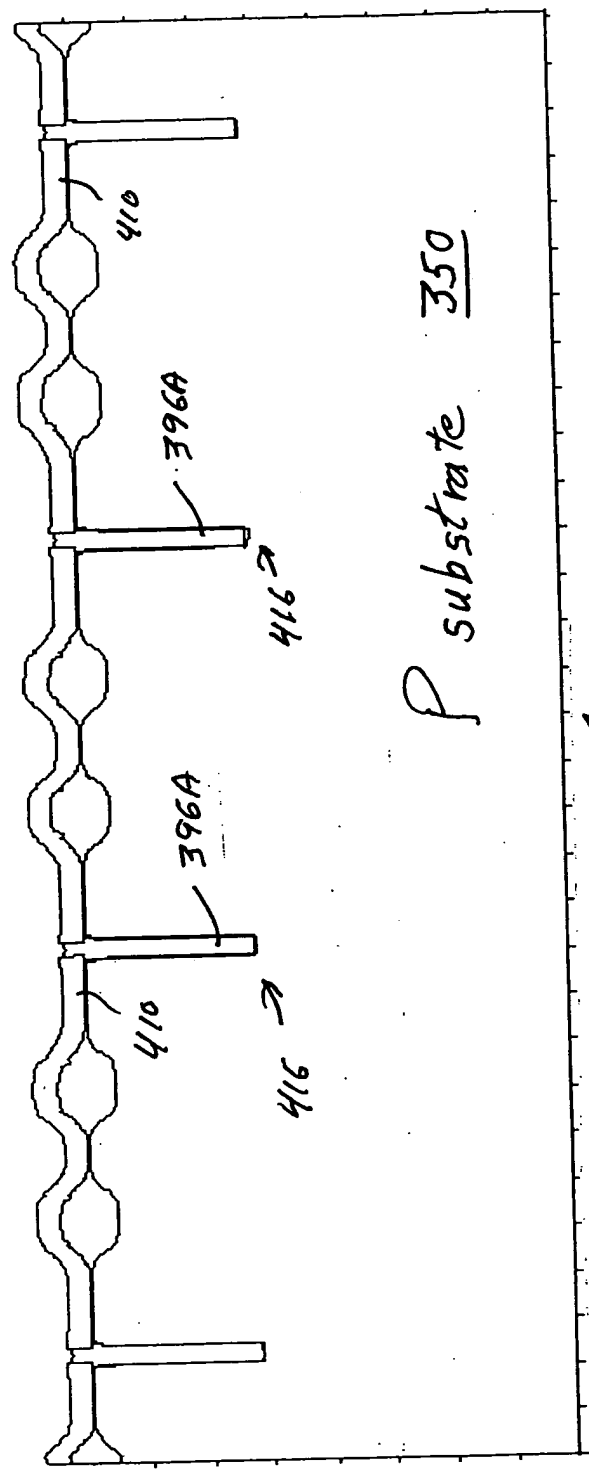
30V Lateral Trench DMOS 308



Polysilicon Etchback - First Layer

Fig. 29D

30V Lateral Trench DMOS 308

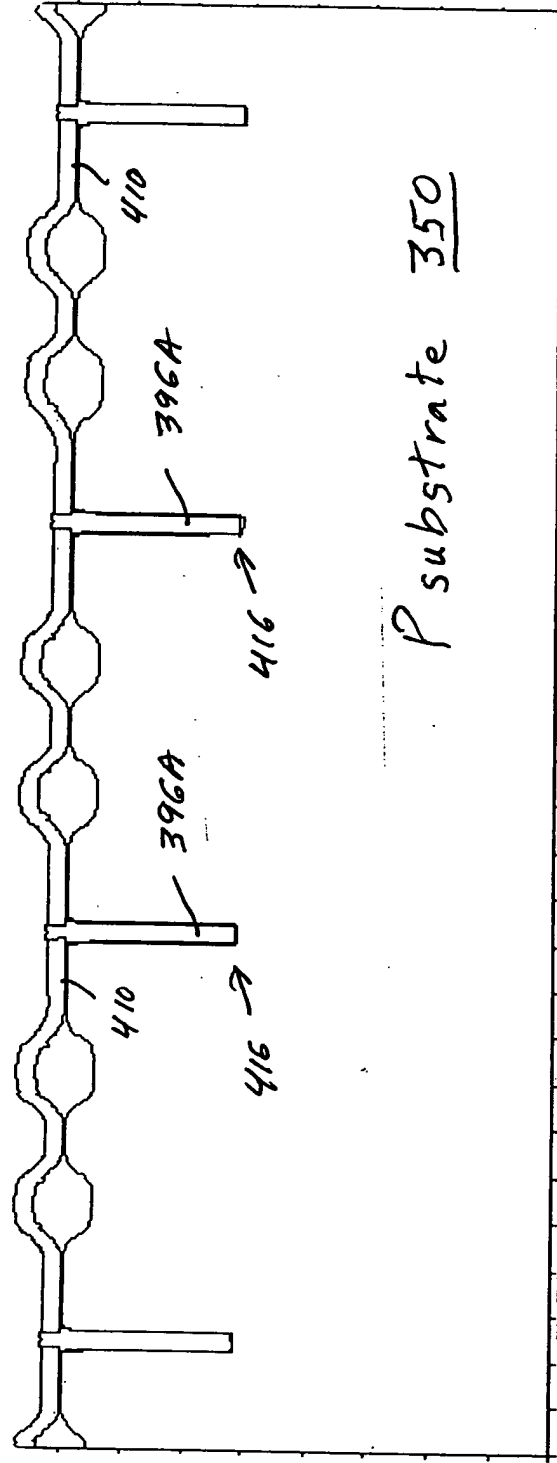


P substrate 350

Hard Mask Removal

Fig. 30 D

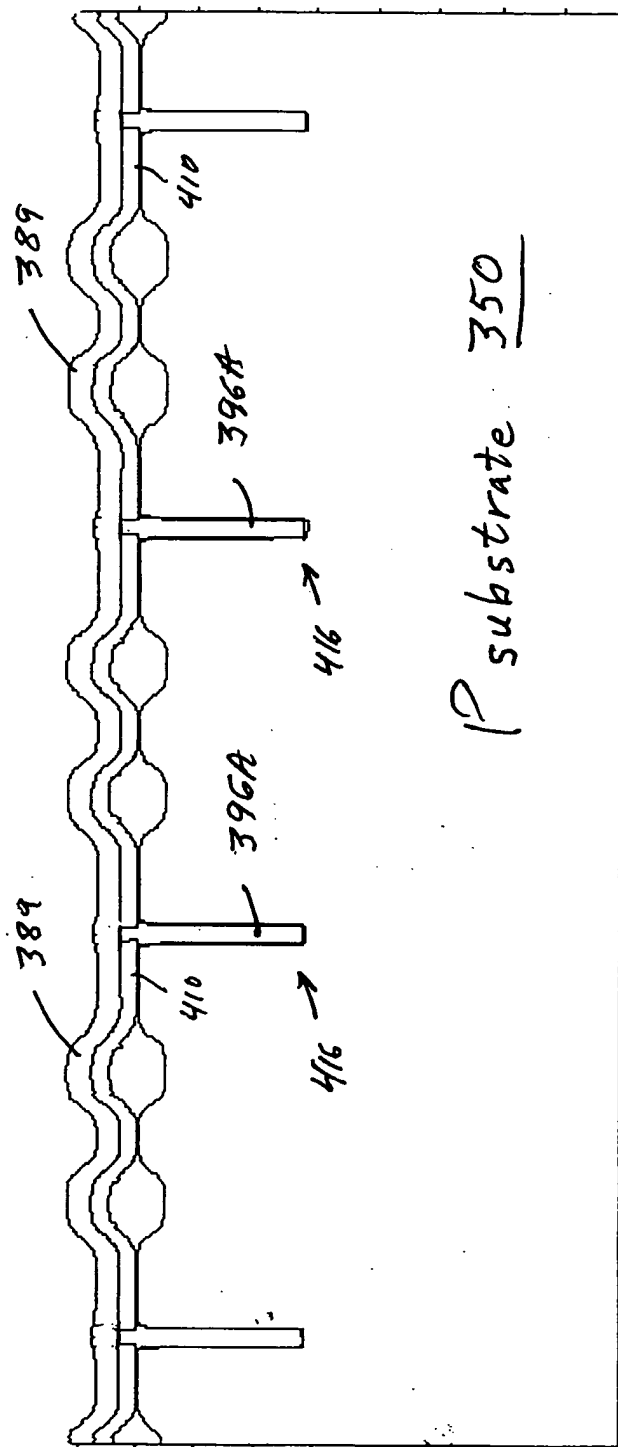
- 30V Lateral Trench DMOS 308



Second Polysilicon Etchback - First Layer
Fig. 31D

30V Lateral Trench DMOS 308

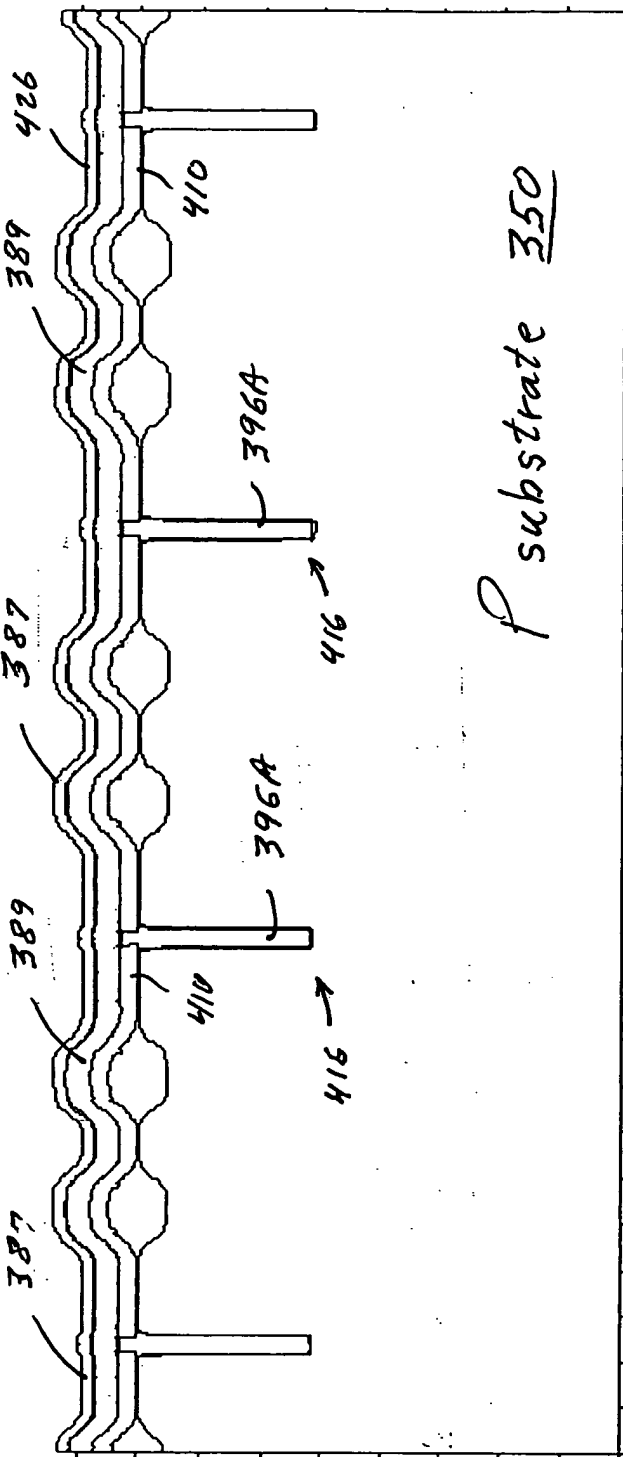
109/219



Polysilicon - Second Layer

Fig. 32D

30V Lateral Trench DMOS 308



P substrate 350

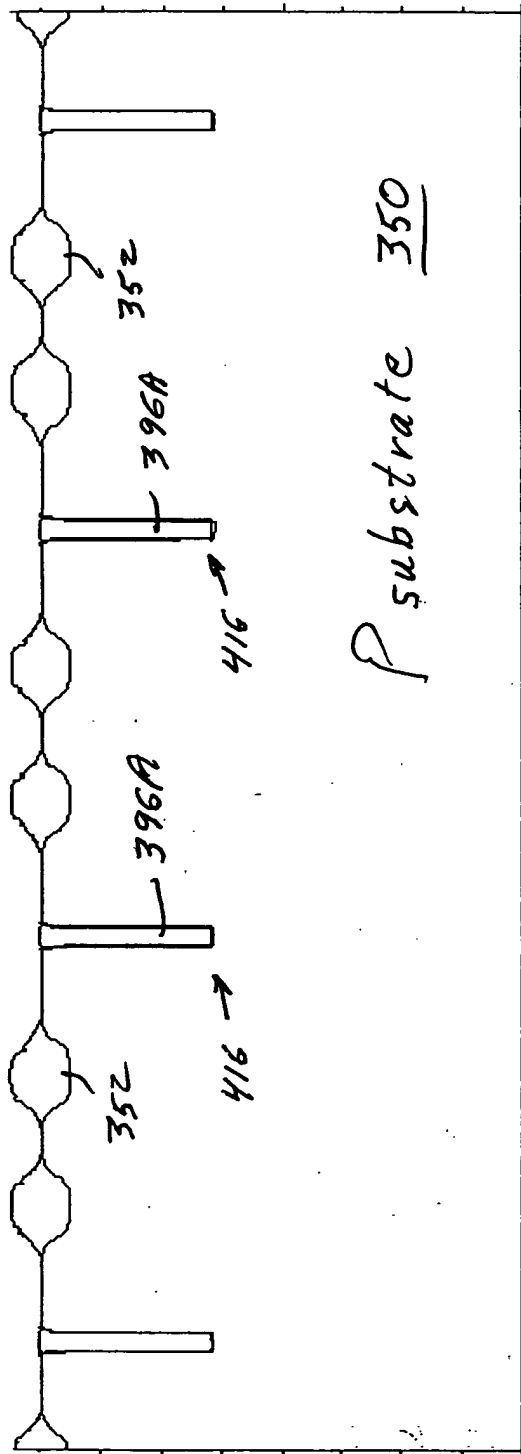
Interlayer Dielectric

Fig 33D

110/219

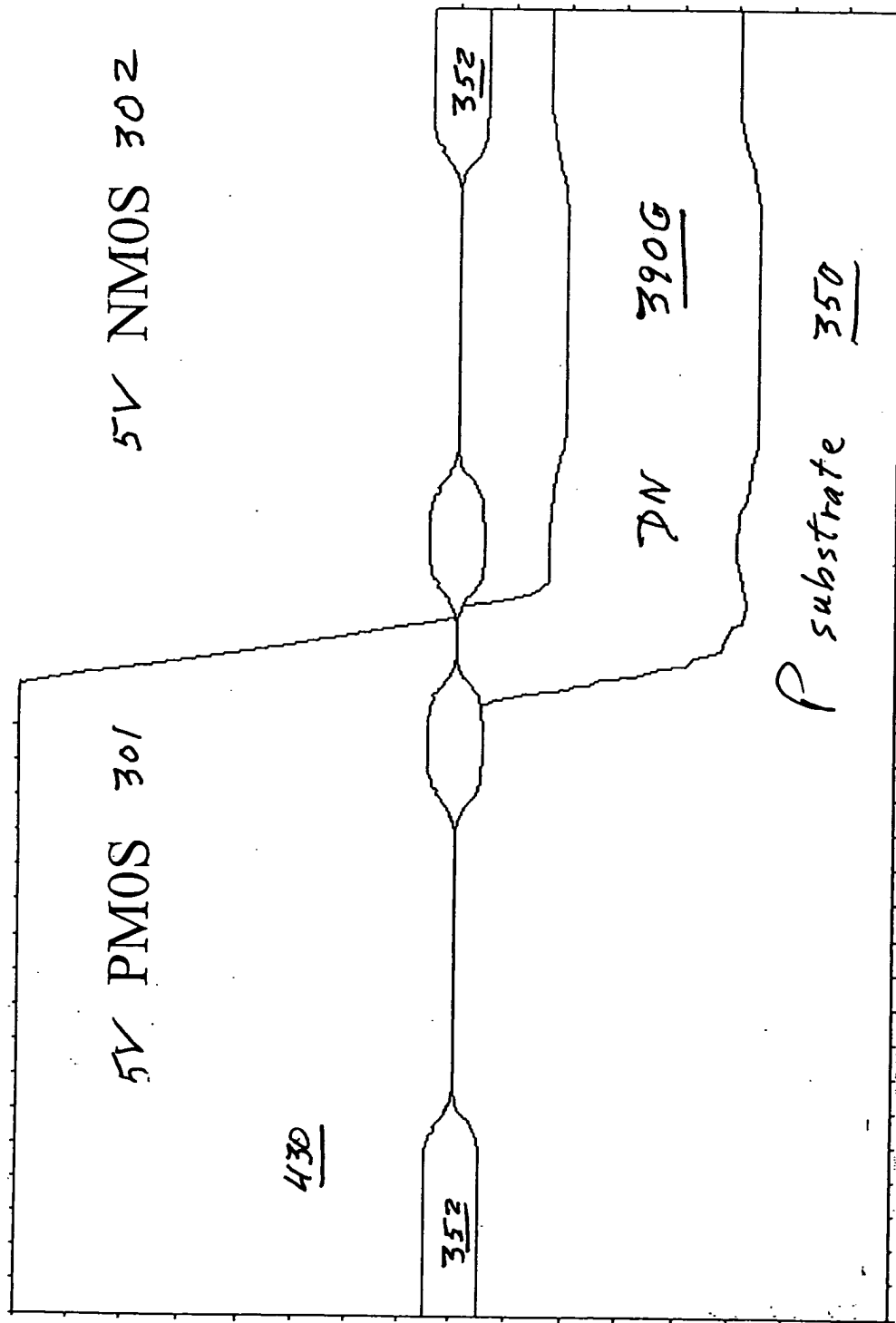
30 V Lateral Trench DMOS 308

111/219



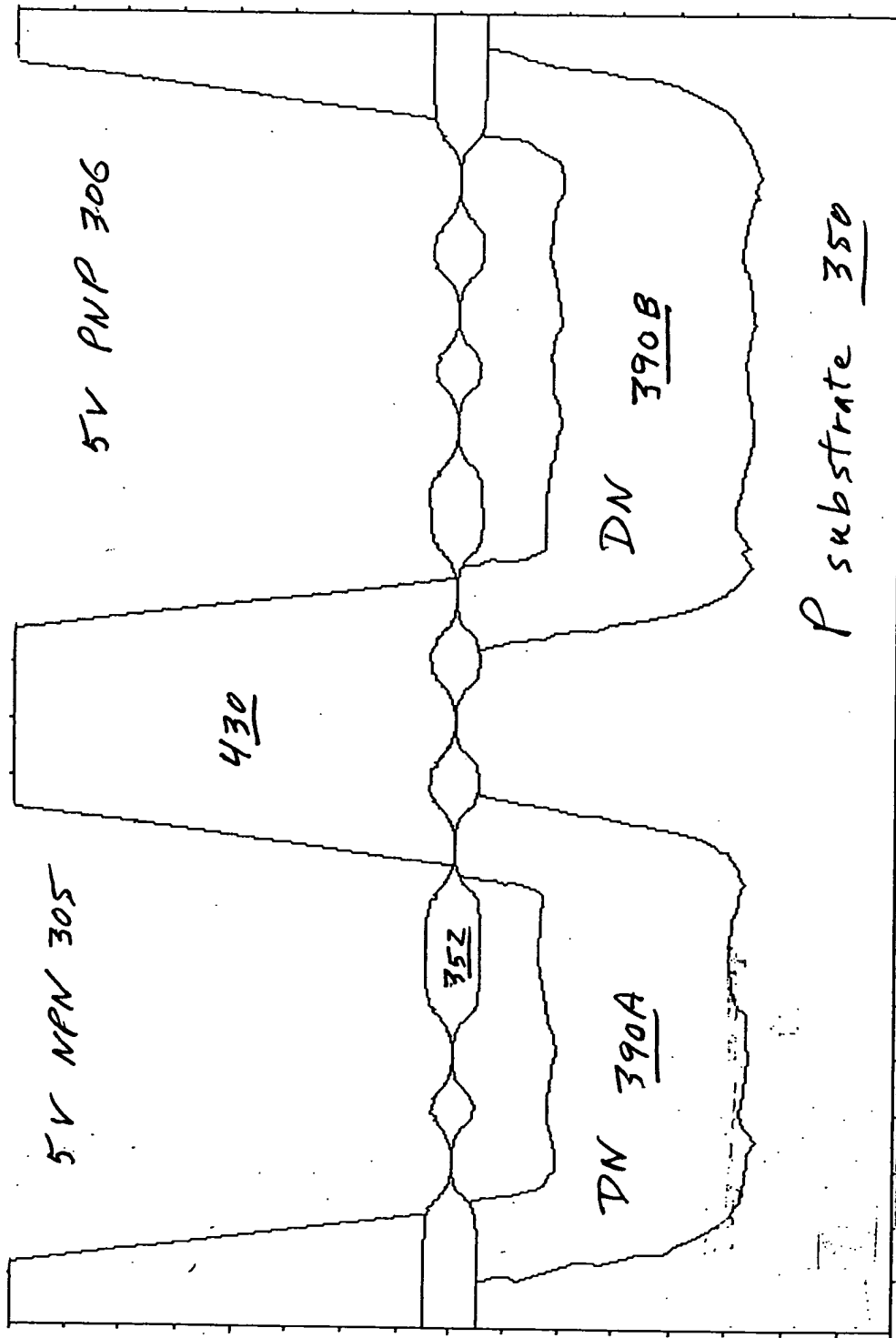
Etch back - Inter-layer Dielectric and Second Poly

Fig. 34D



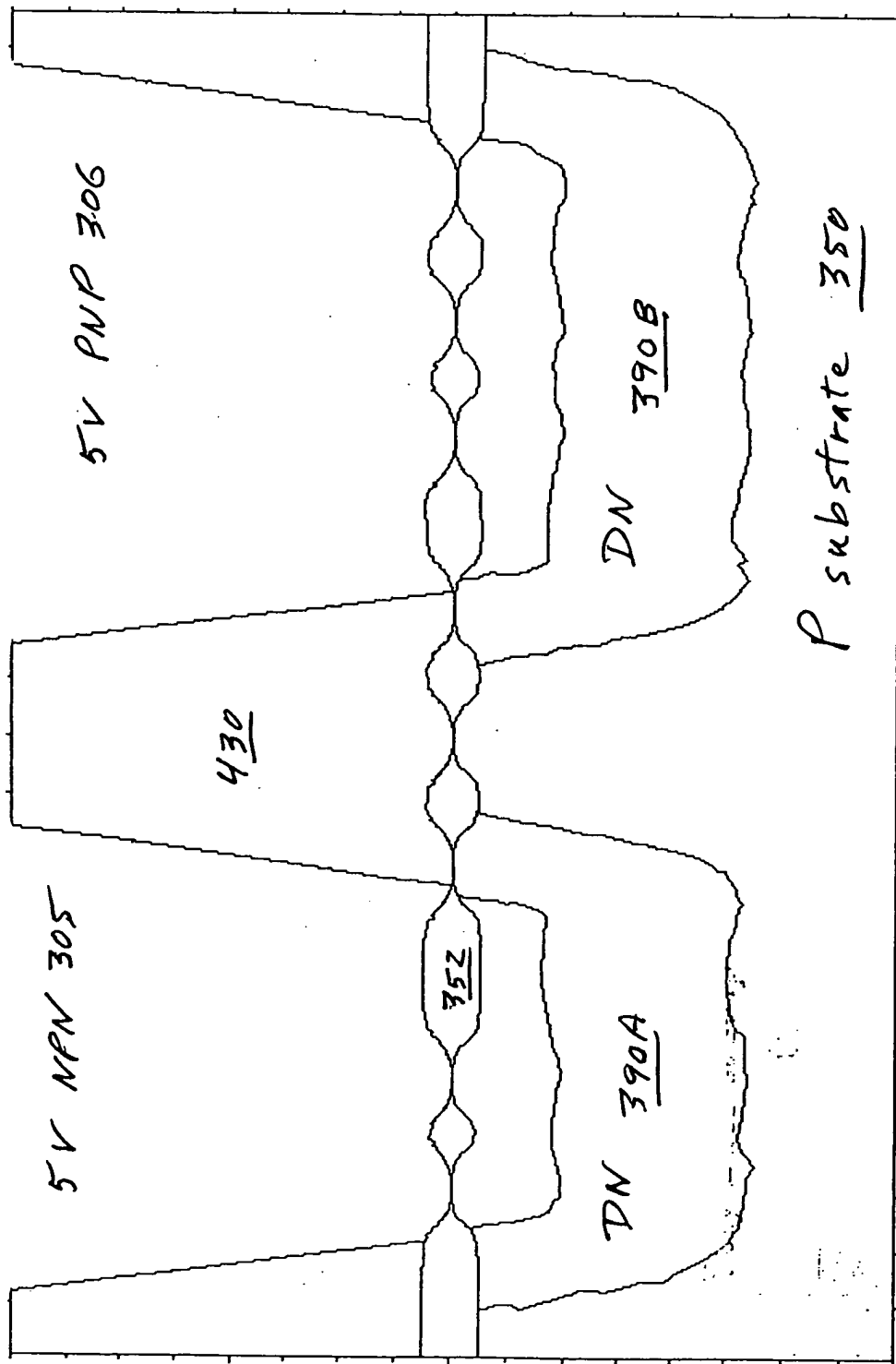
Deep N Mask and Implant
Fig. 35A

112/219

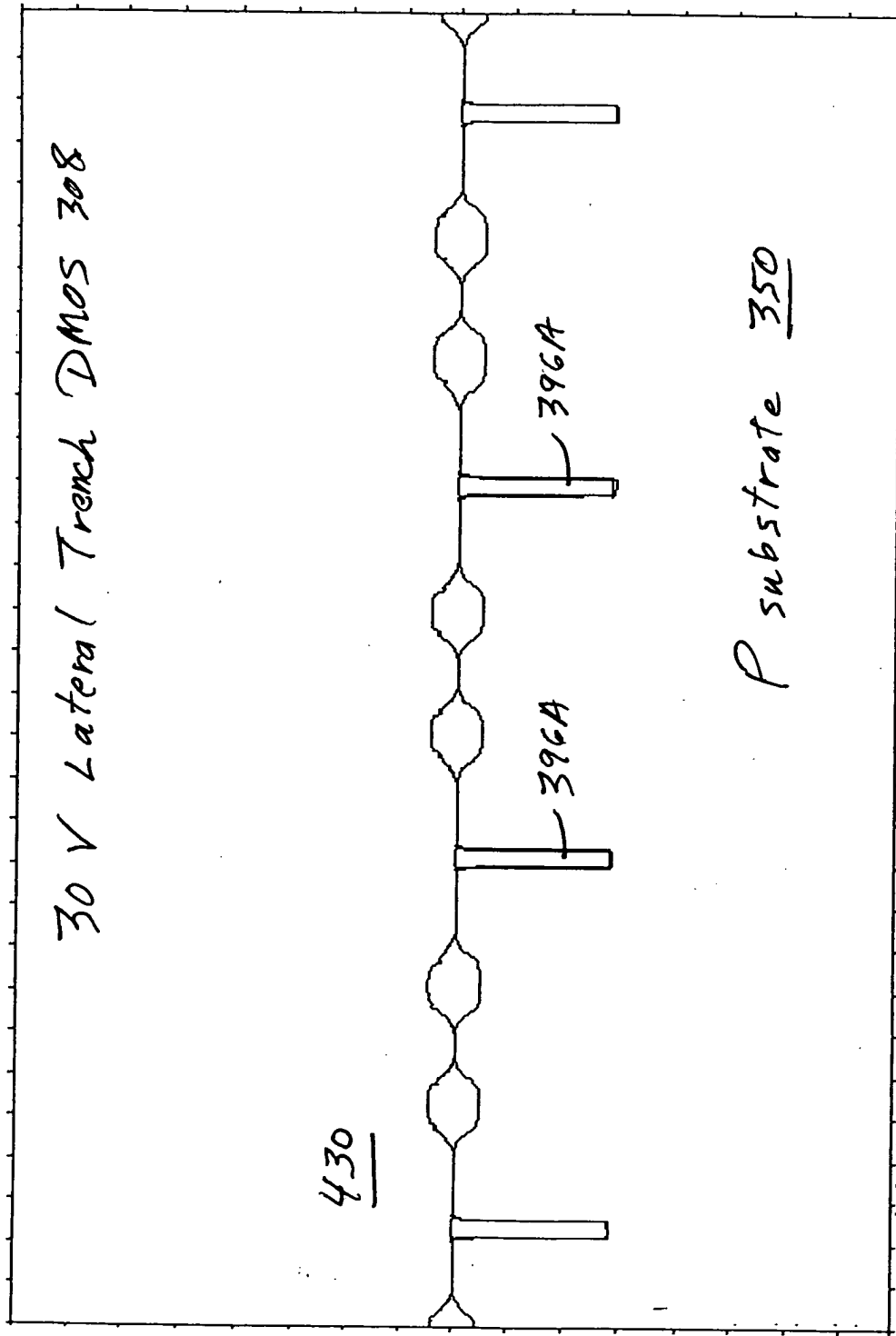
High F_T LayoutDeep N Mask and Implant
Fig 351B

11/4/219

Conventional Layout



Deep N Mask and Implant
Fig. 35C

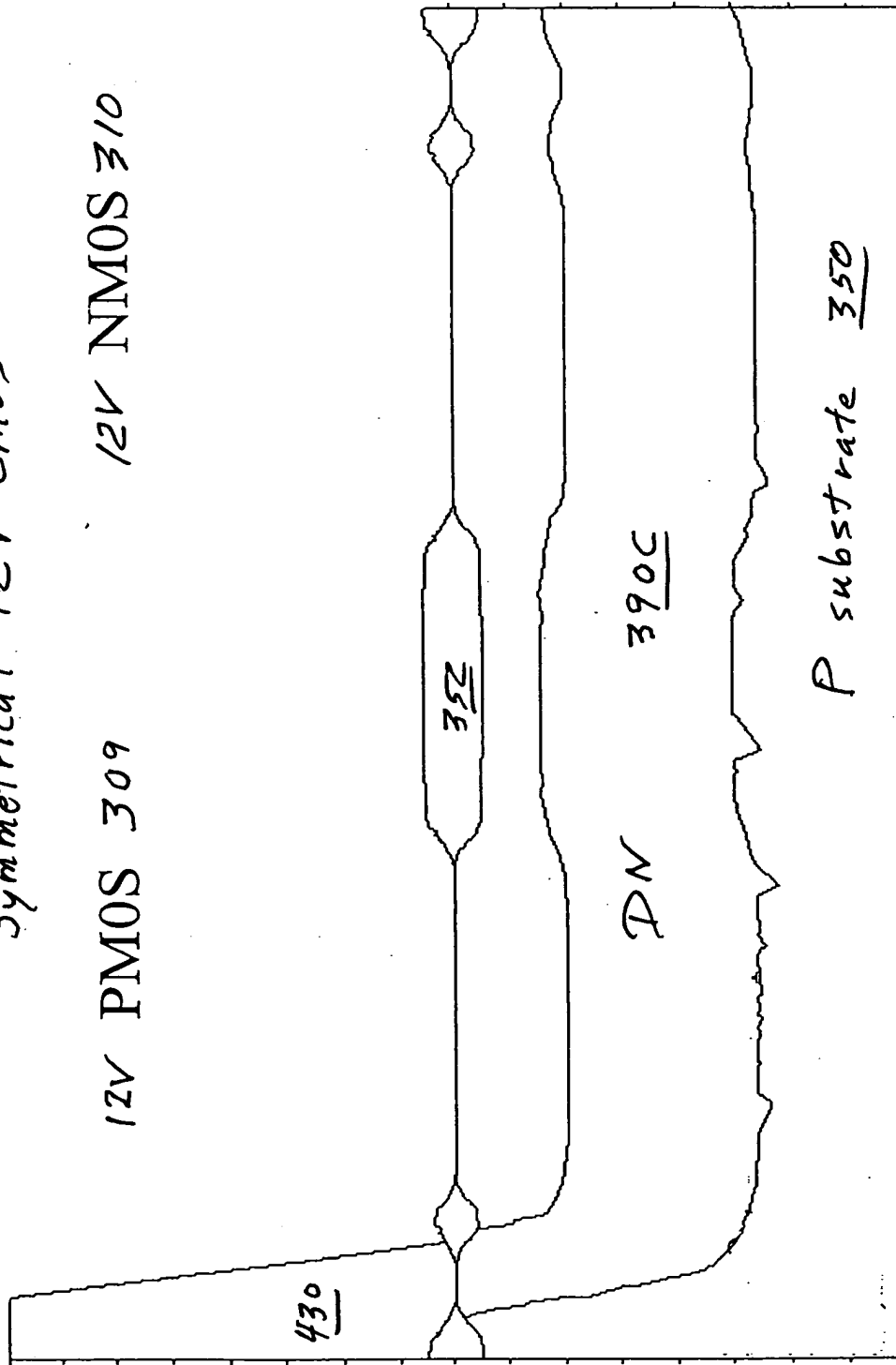


Deep N Mask and Implant
Fig. 35D

116/219

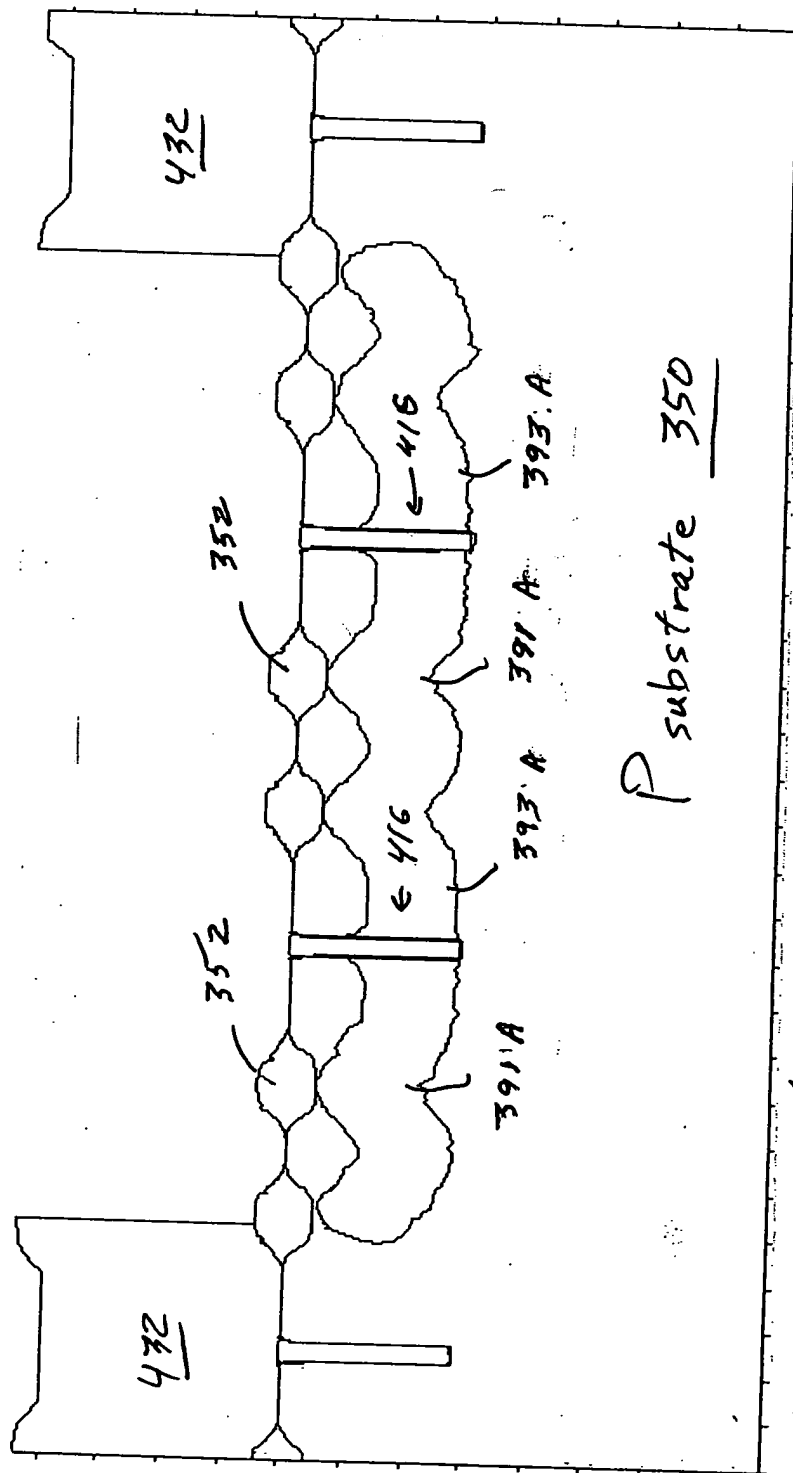
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Deep N Mask and Implant
Fig. 35E

30 V Lateral Trench DMOS 308



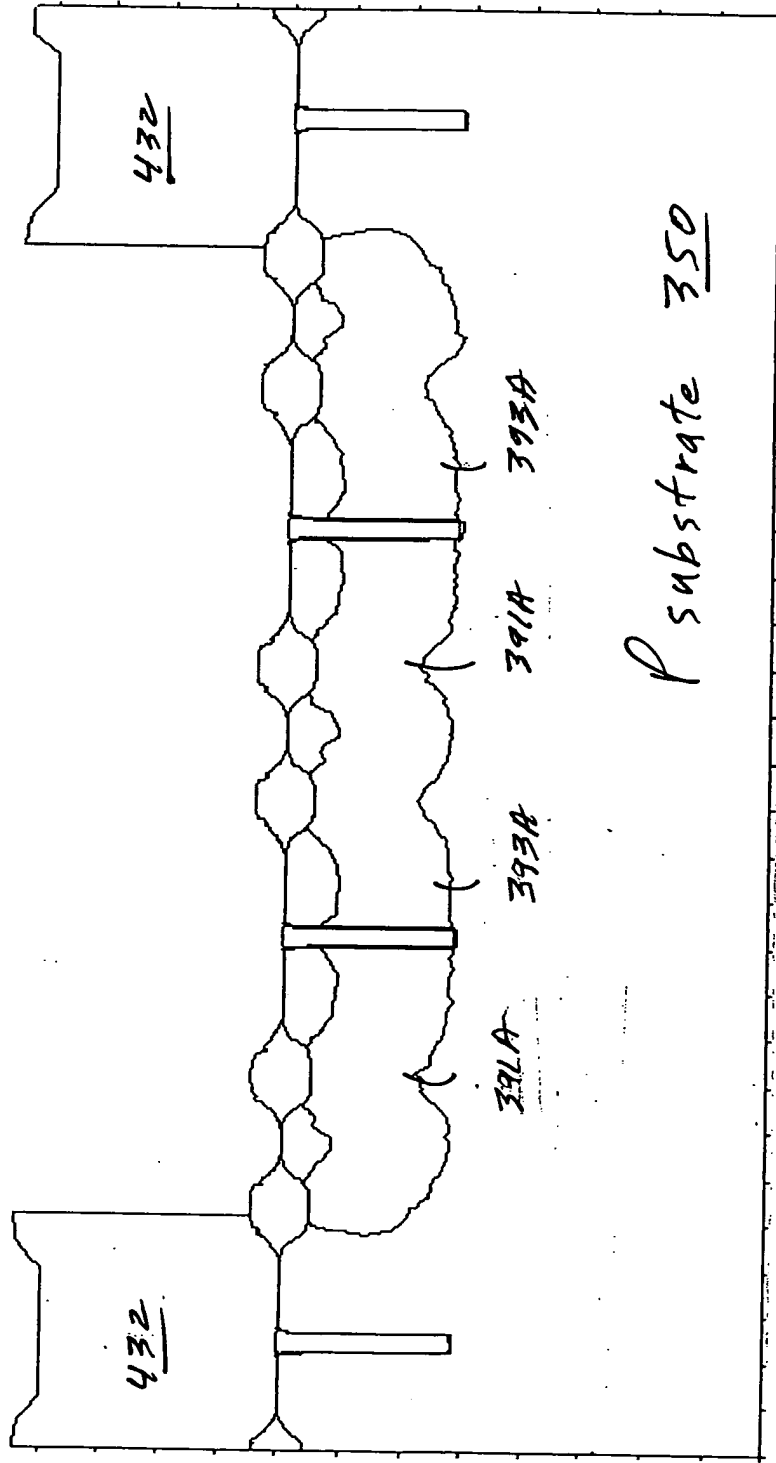
N Drift Implant - First Stage

Fig. 36D

117/219

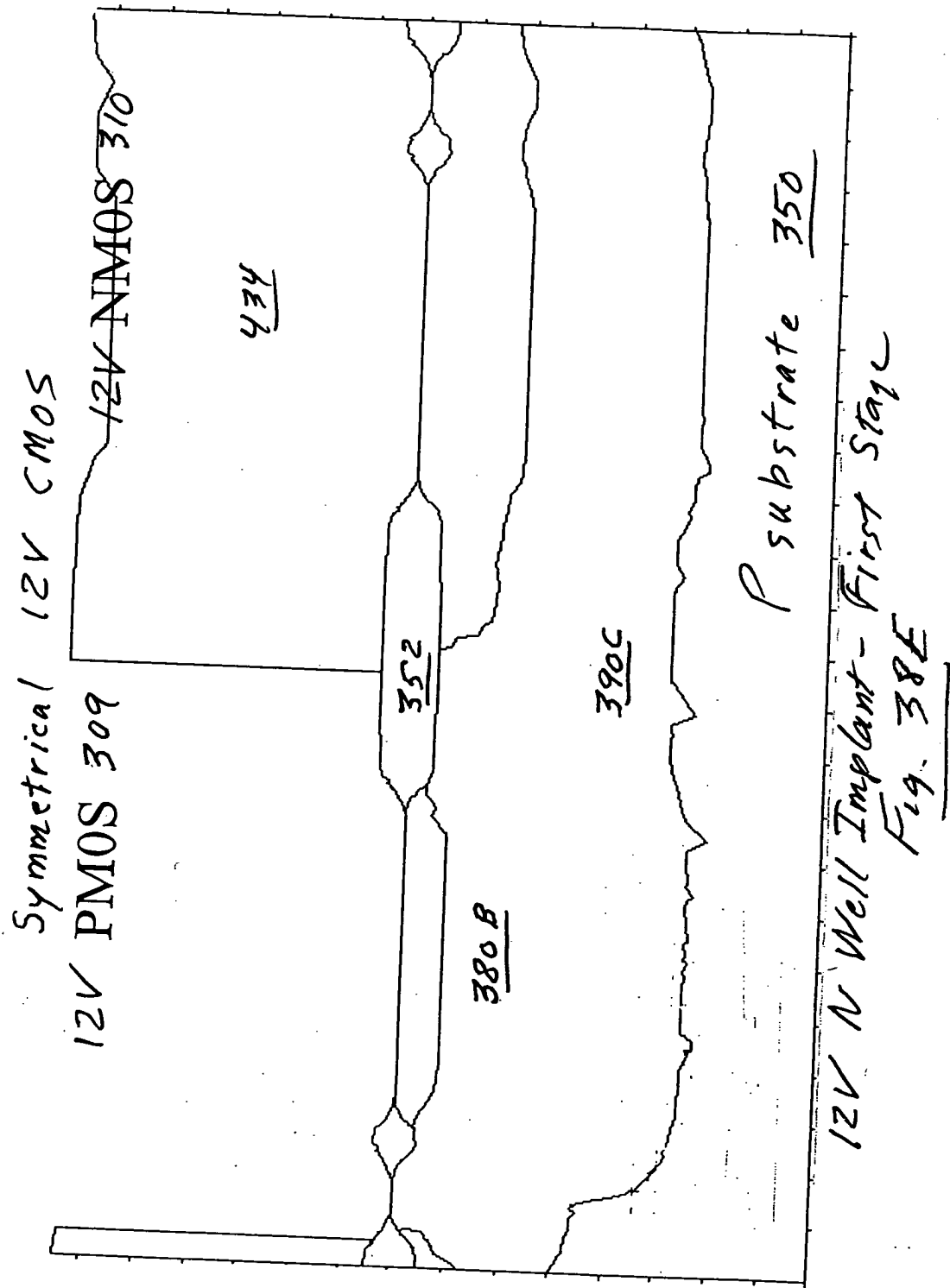
118/219

30V Lateral Trench DMOS 308

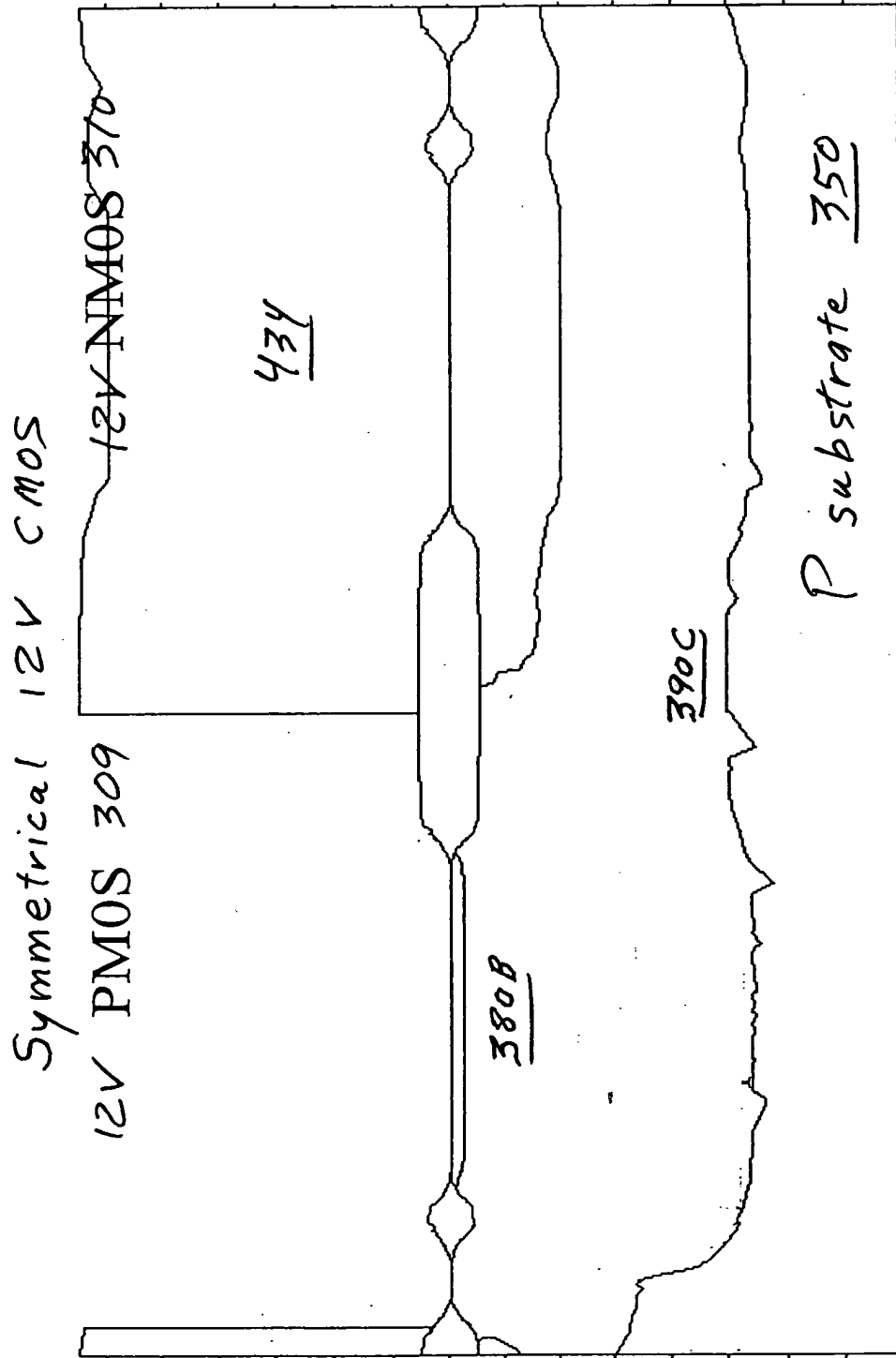


N Drift Implant - Second Stage
Fig. 37D

119/219



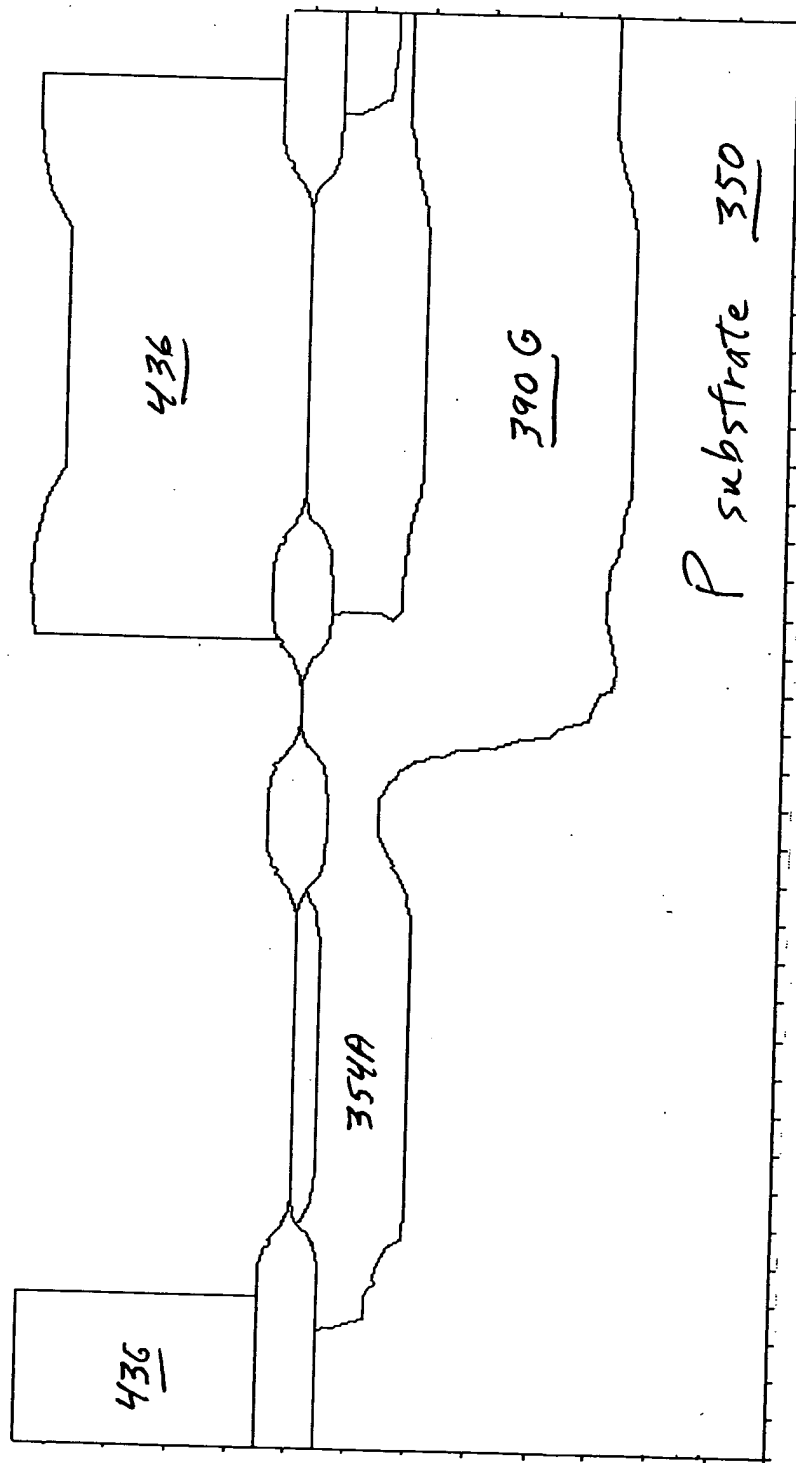
120/219



12V N Well Implant - Second Stage

Fig. 39E

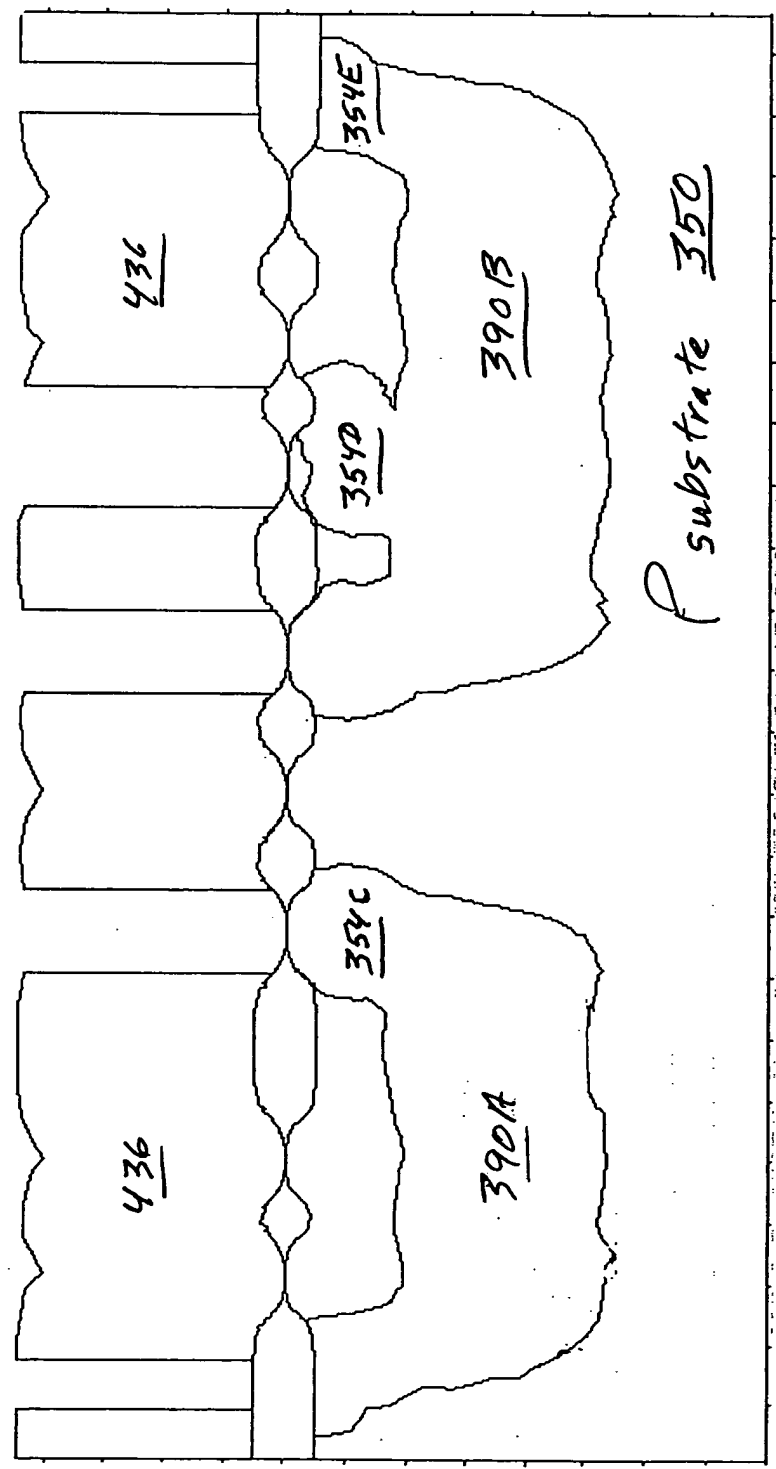
5V PMOS 301 5V NMOS 302



5V N Well Implant - First Stage

Fig. 40A

High F_T Layout
5V NPN 305 5V PNP 306

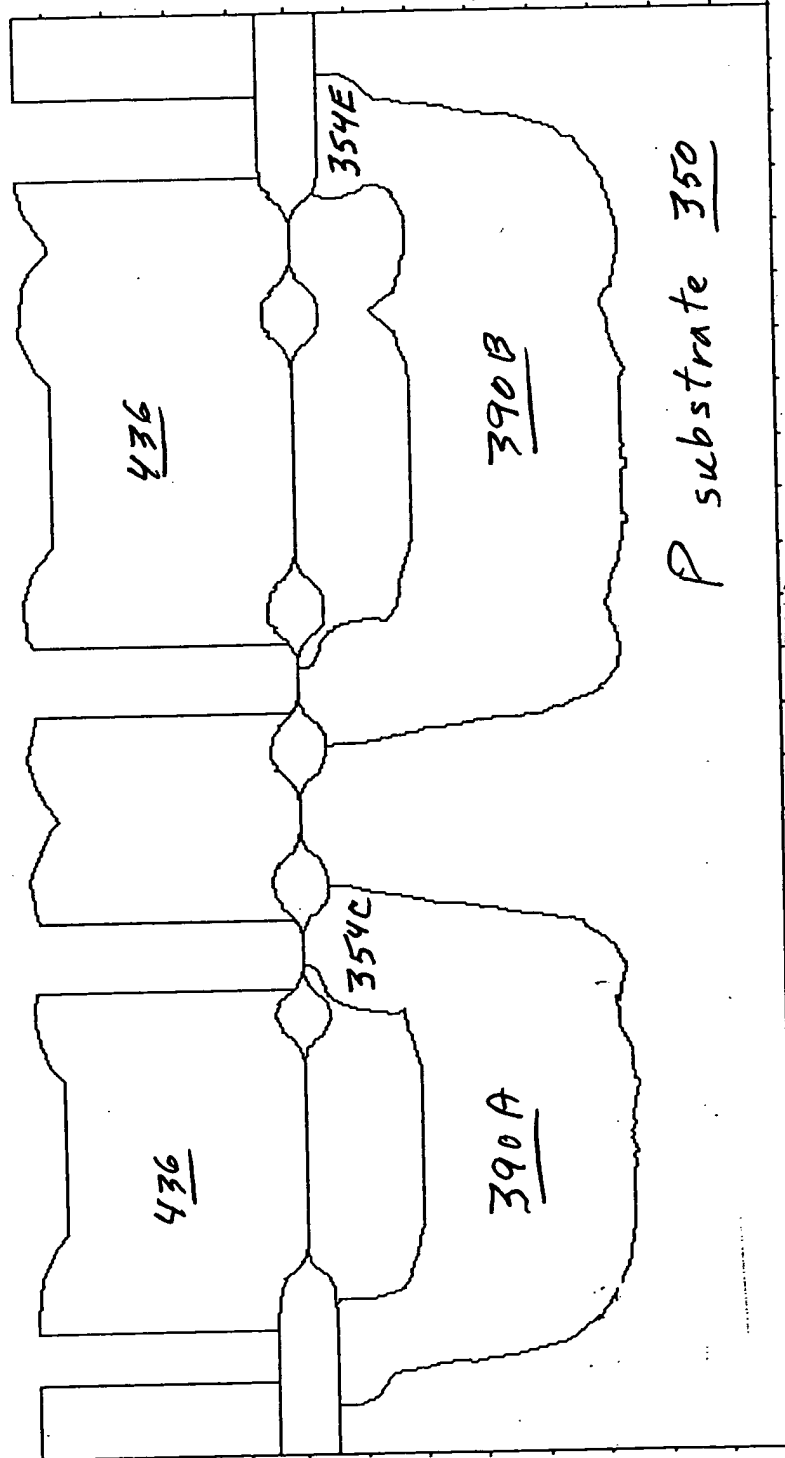


5V N Well Implant - First Stage
Fig. 40B

Conventional Layout

5V PNP

5V NPN

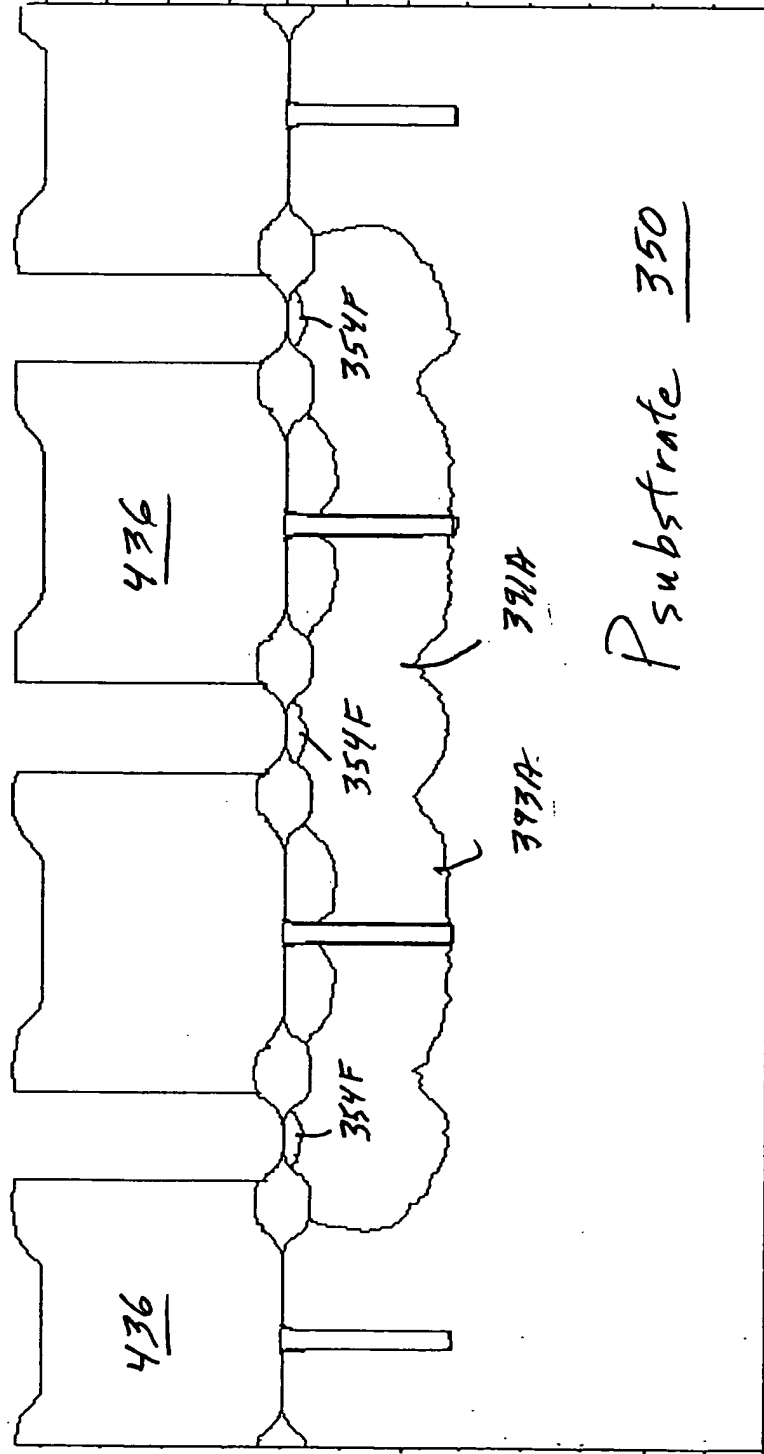


5V N Well Implant - First Stage

Fig. 40C

124/219

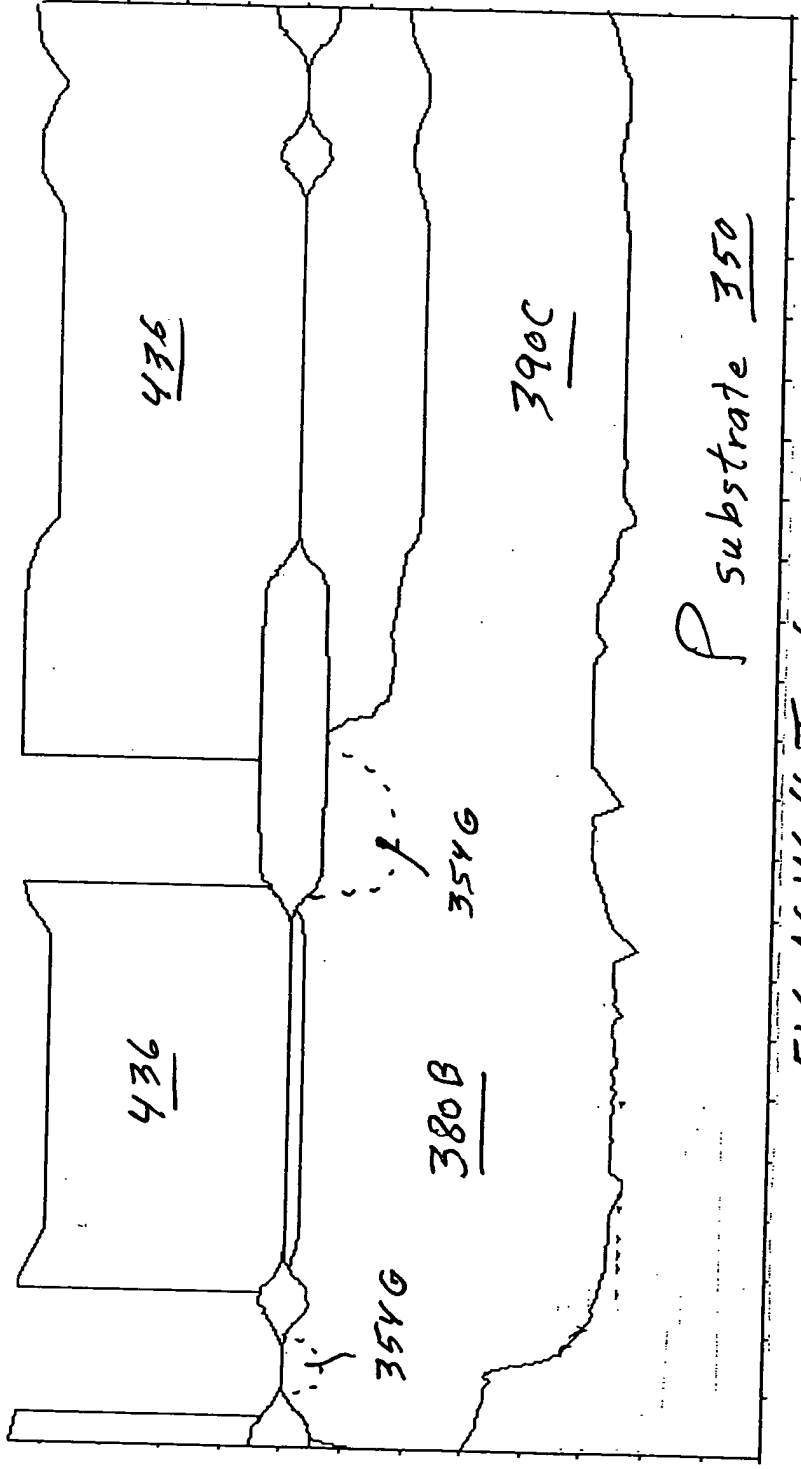
30V Lateral Trench DMOS 308



5V N Well Implant - First Stage

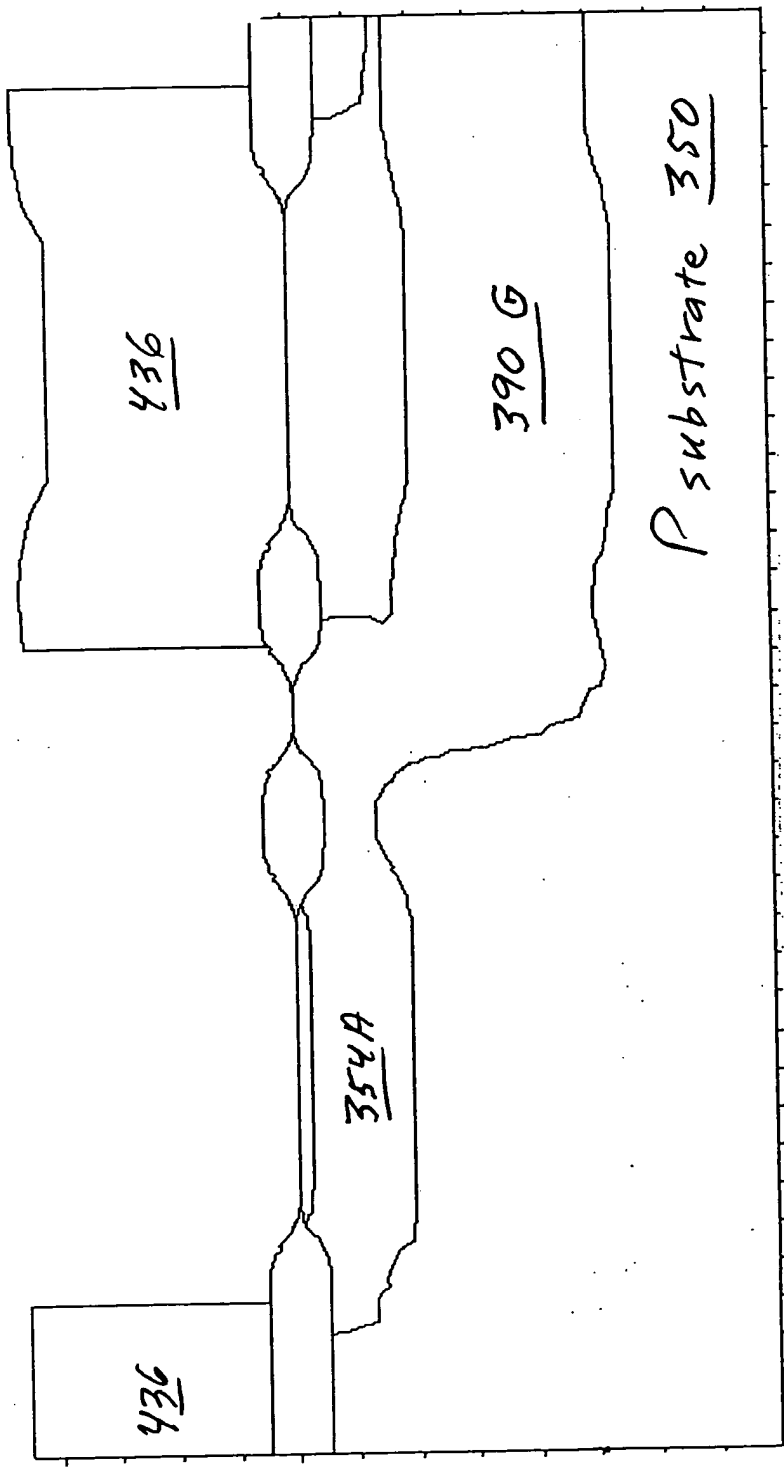
Fig 40D

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



5V N Well Implant - First Stage
Fig 40E

5V PMOS 301 5V NMOS 302

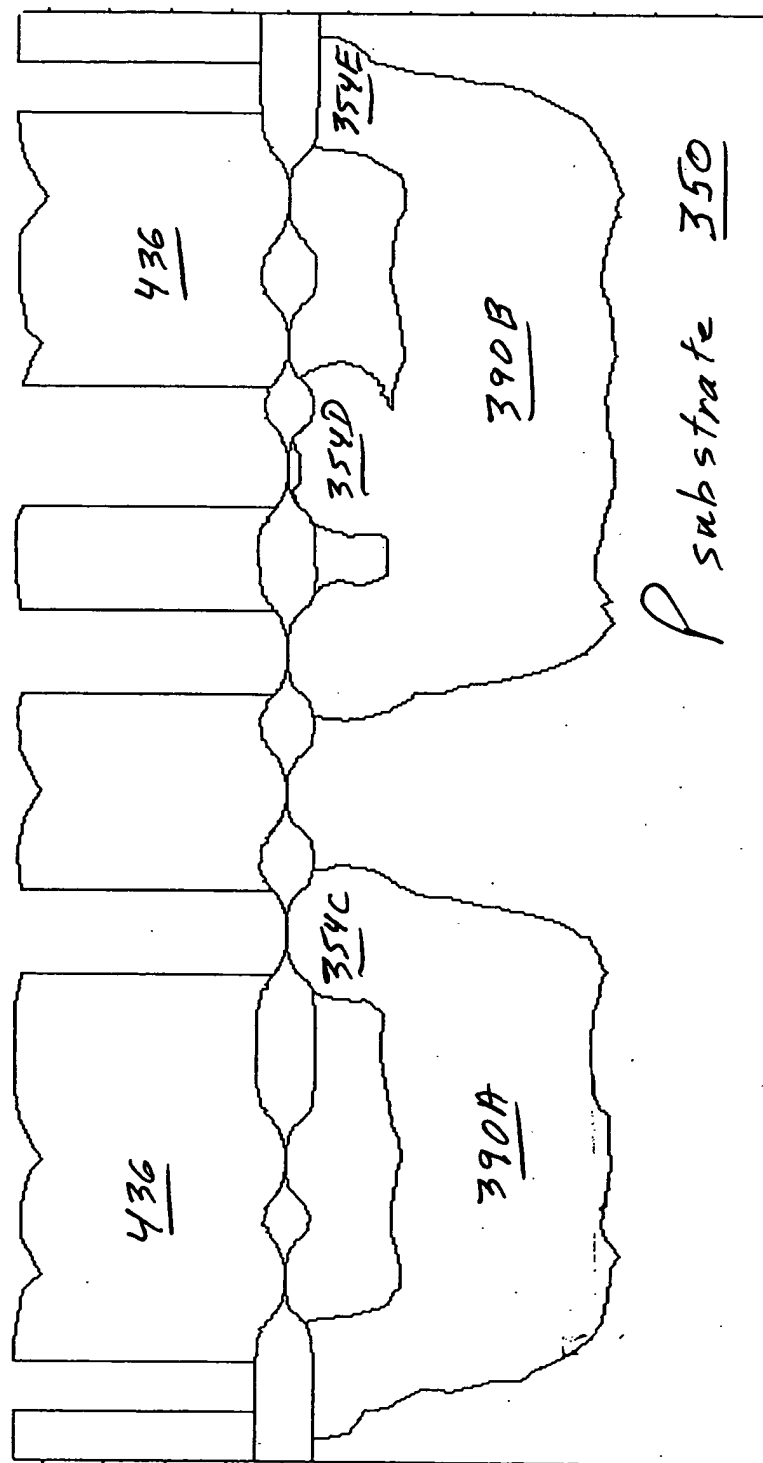


5V NWell Implant - Second Stage
Fig. 41A

High F_T Layout

5V NPN 305

5V PNP 306



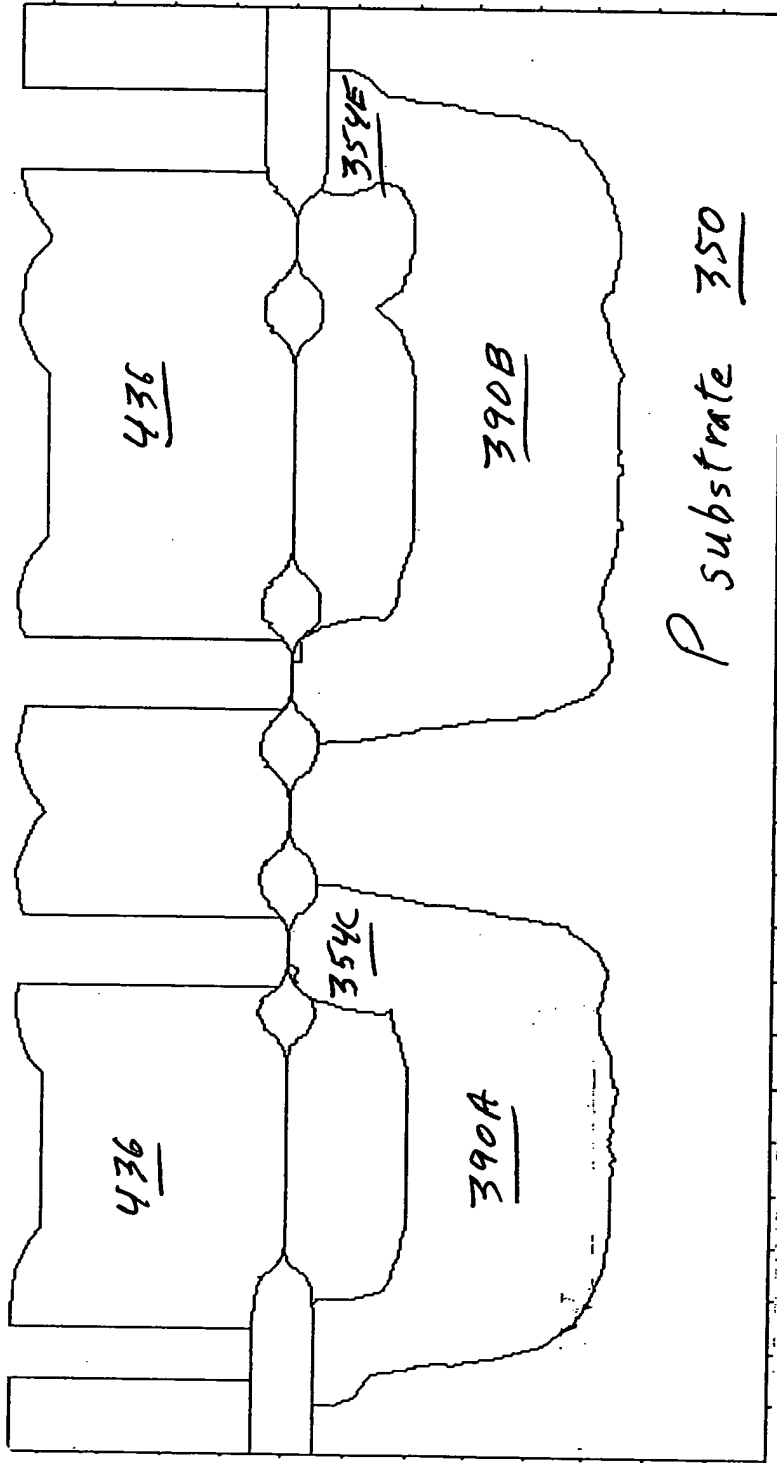
5V N Well Implant - Second Stage

Fig. 41B

Conventional Layout

5V NPN

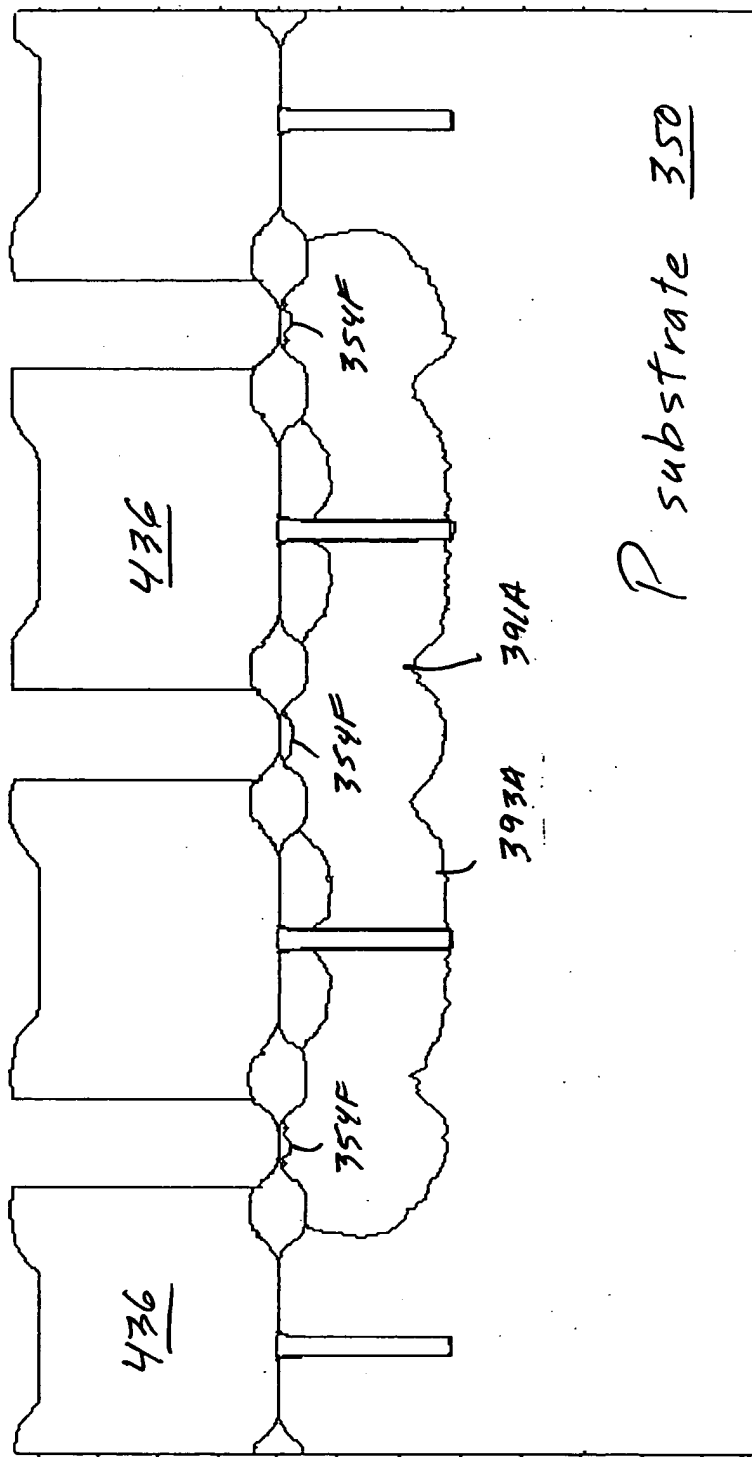
5V PNP



5V N Well Implant - Second Stage

Fig. 41C

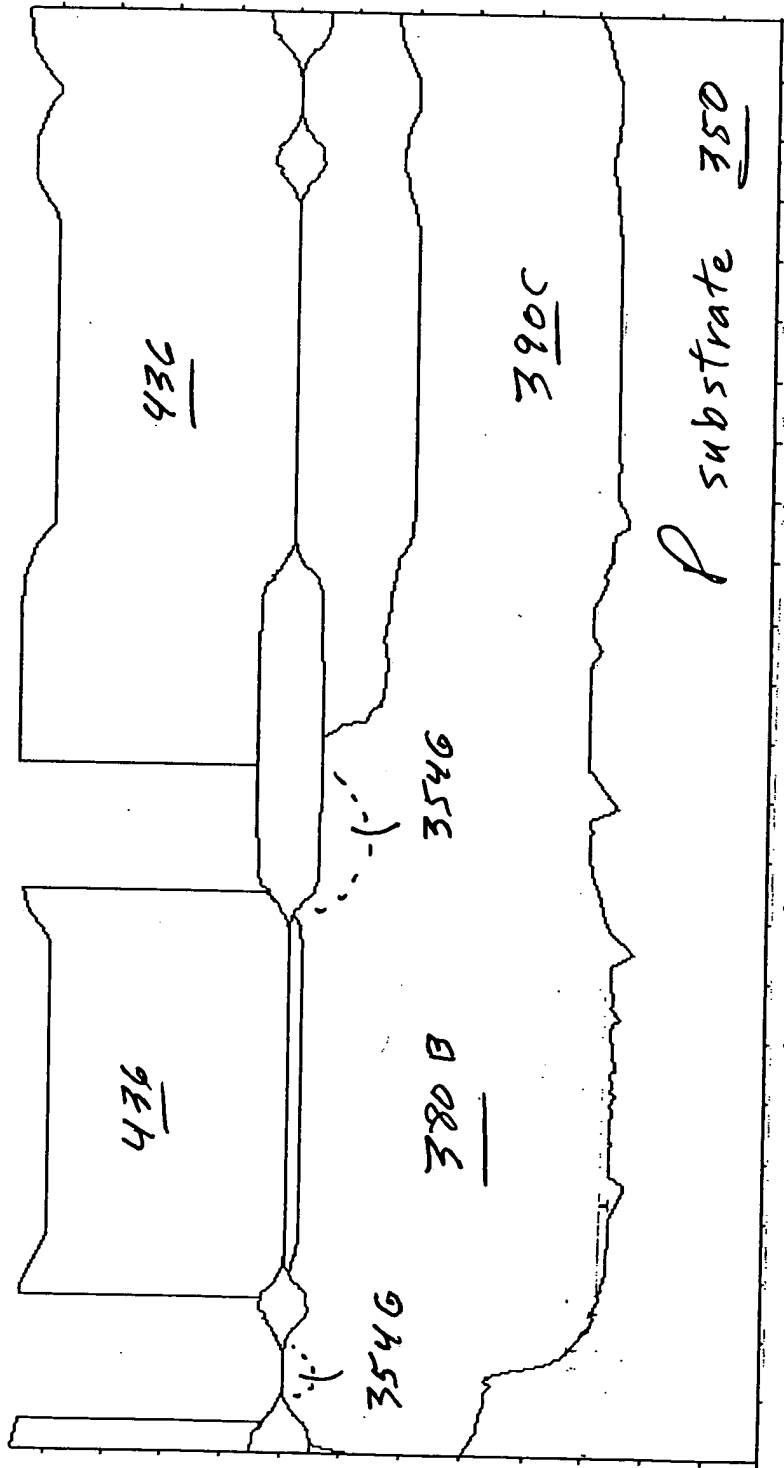
30V Lateral Trench DMOS 308



5V NWell Implant - Second Stage

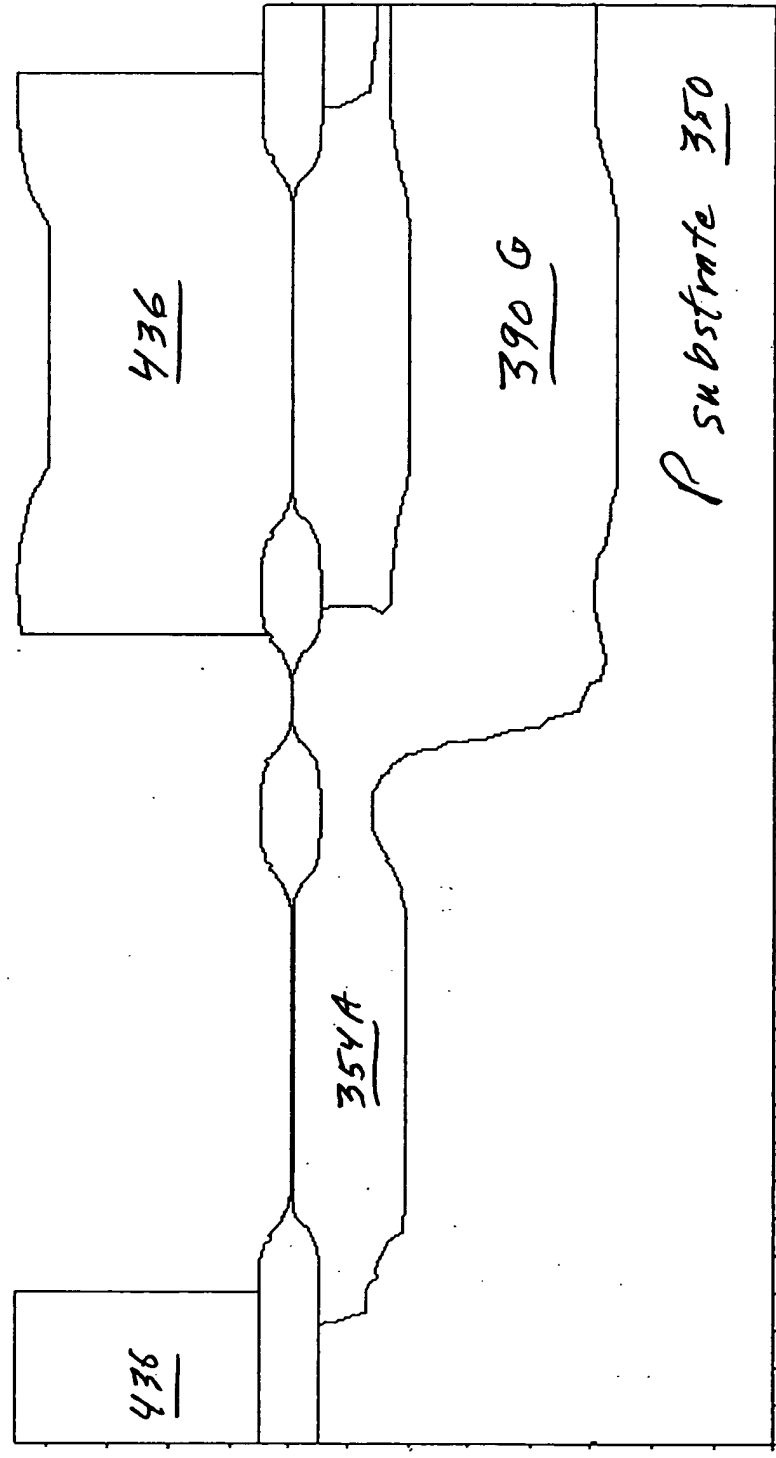
Fig. 41D

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



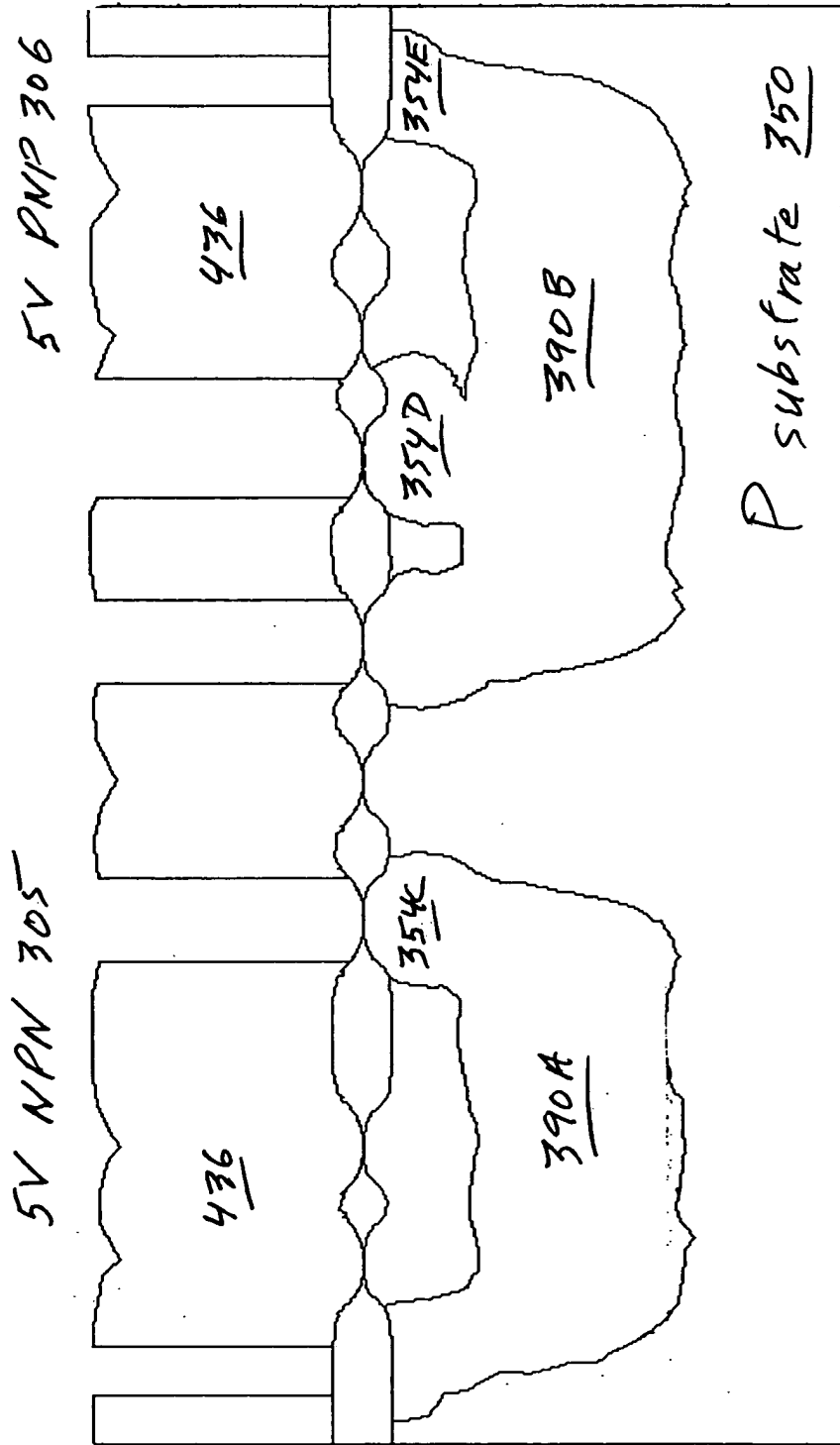
5V NWell Implant - Second Stage
Fig. 41E

5V PMOS 301 5V NMOS 302



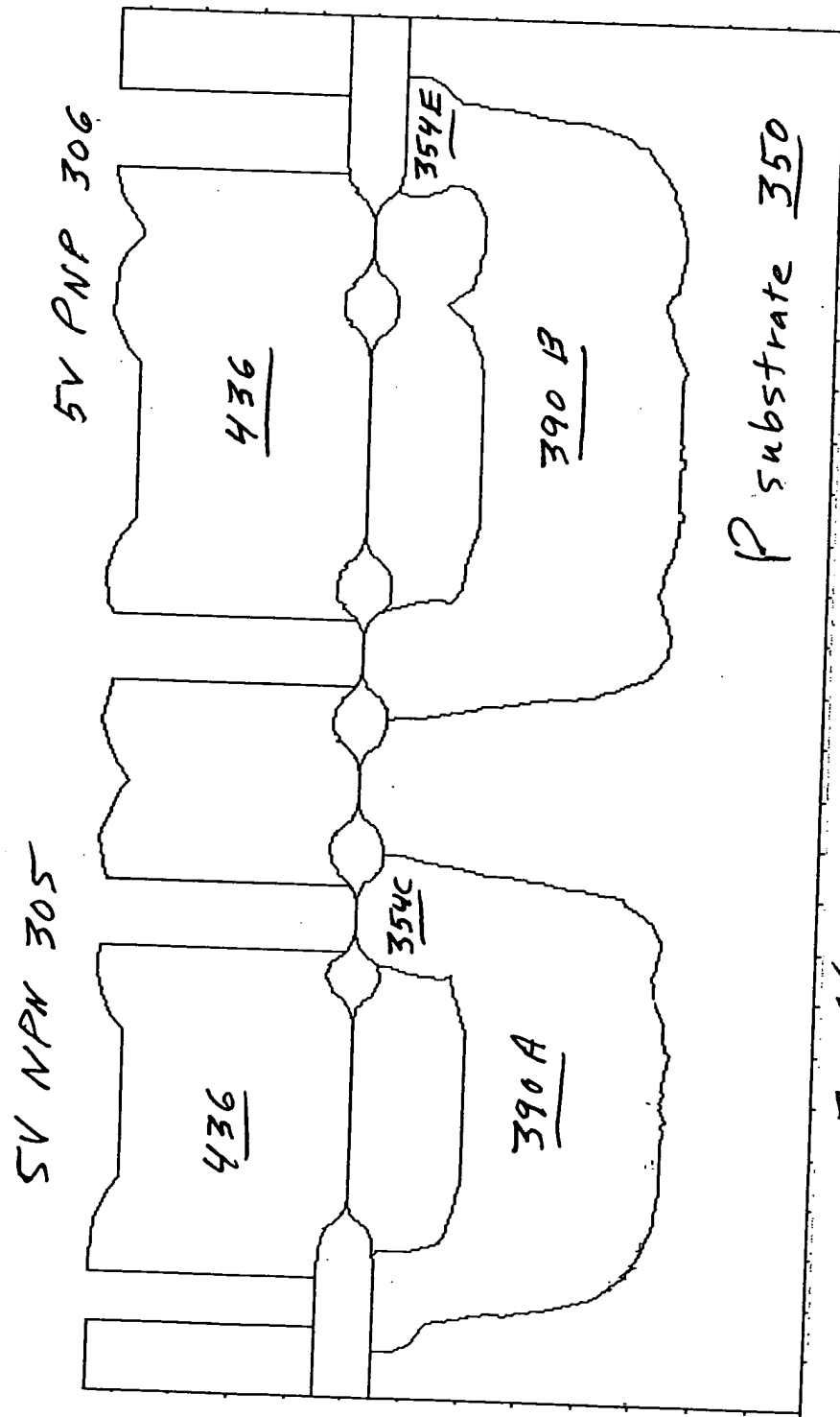
5V N Well Implant - Third Stage
Fig. 42A

High F_T Layout



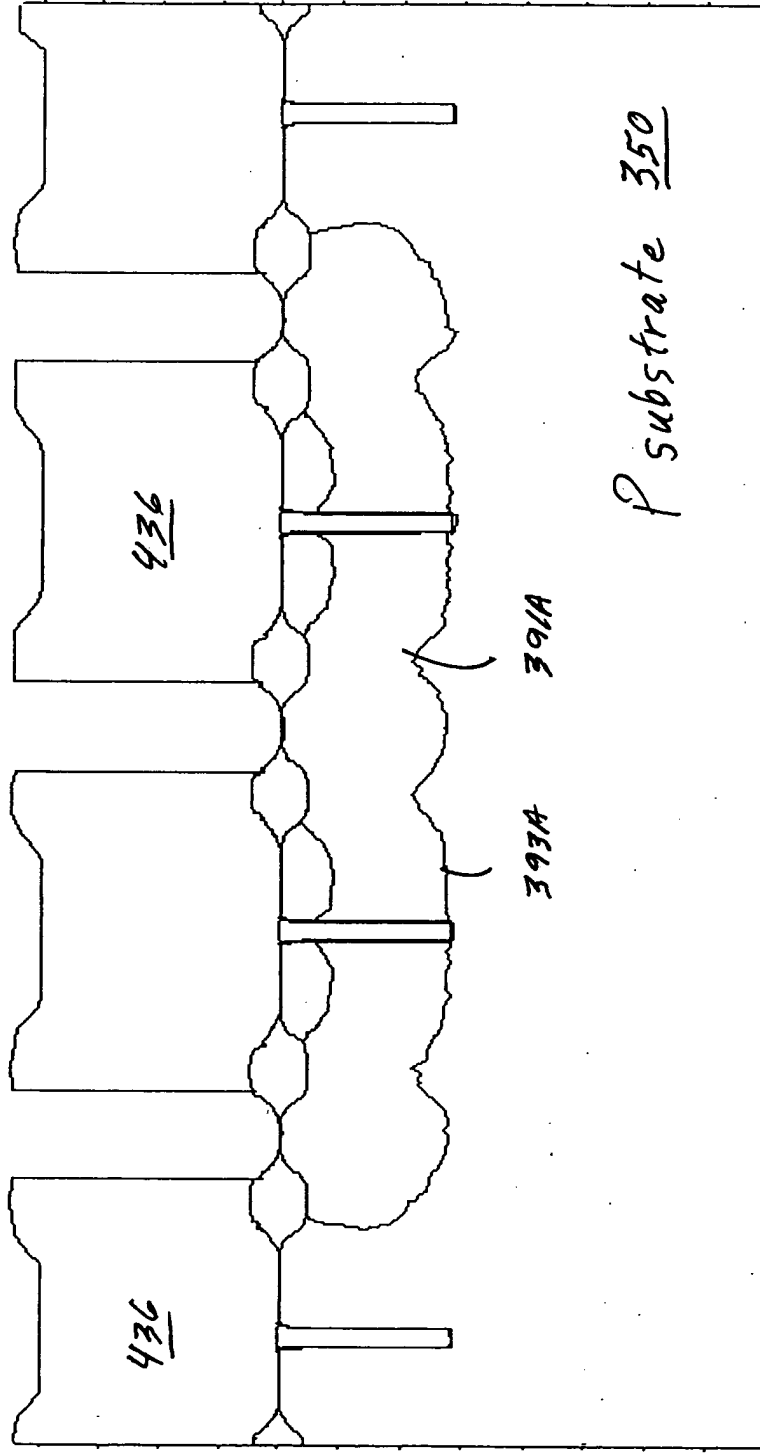
5V NWell Implant - Third Stage
Fig. 42B

Conventional Layout



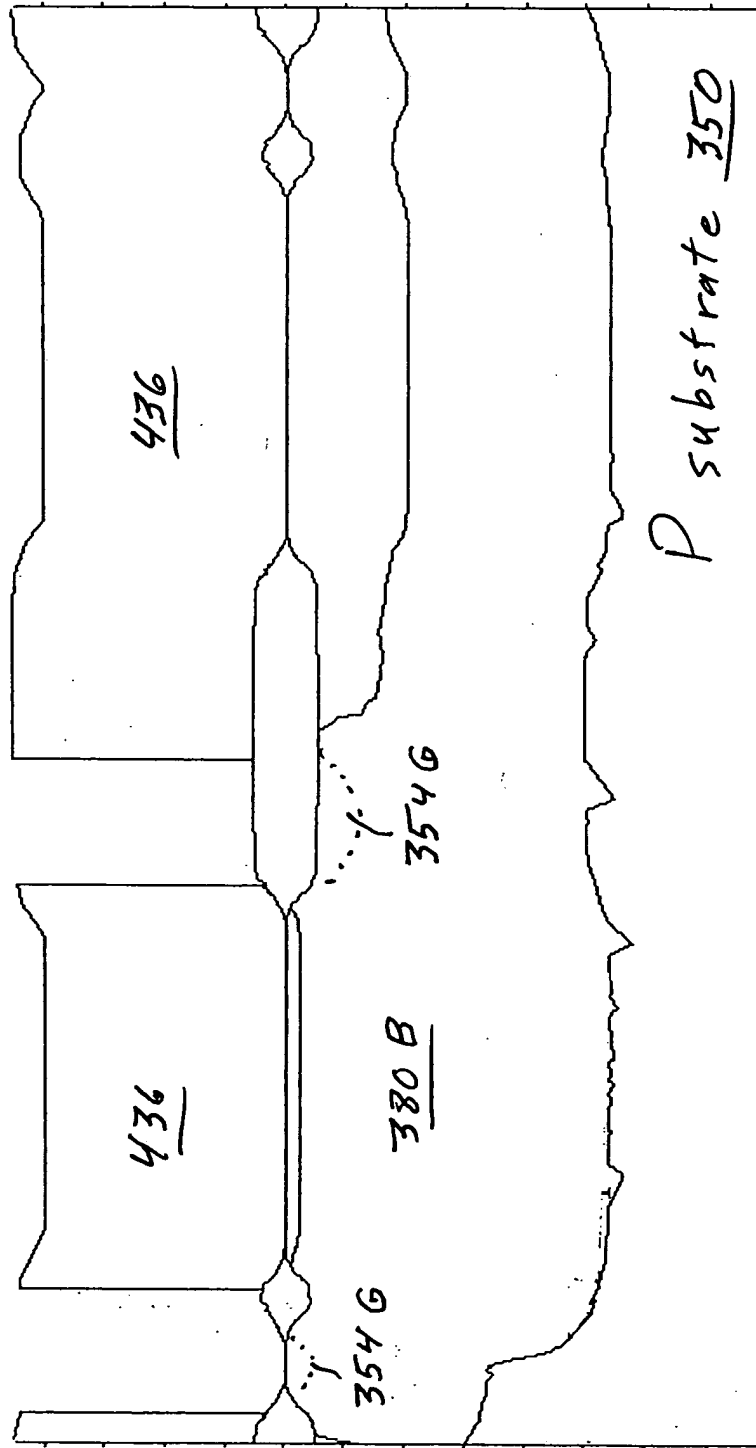
5V N Well Implant - Third Stage
Fig. 42C

30V Lateral Trench DMOS 308



5V N Well Implant - Third Stage
Fig. 42D

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



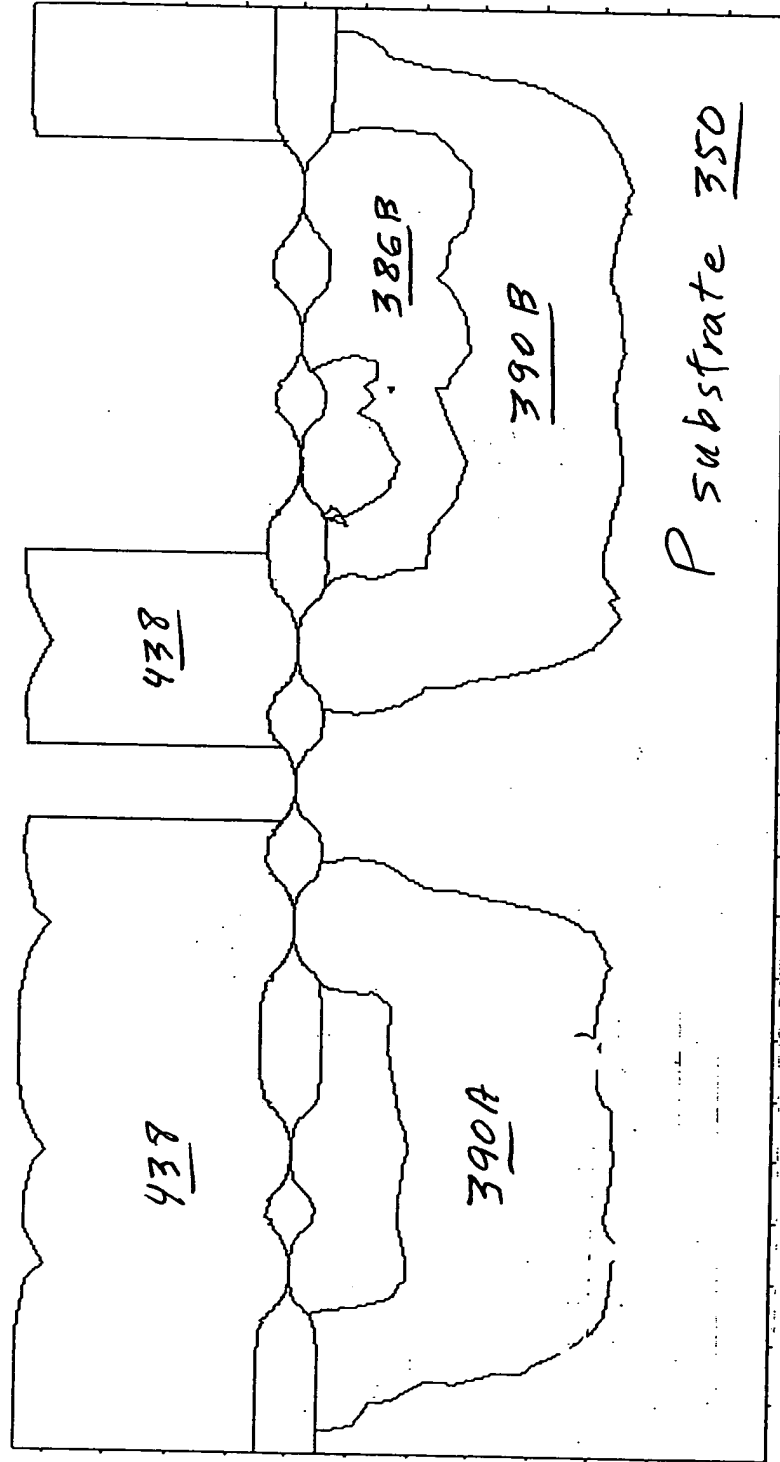
5V N Well Implant - Third Stage
Fig. 42 E

136/219

High F_T Layout

5V NPN 305

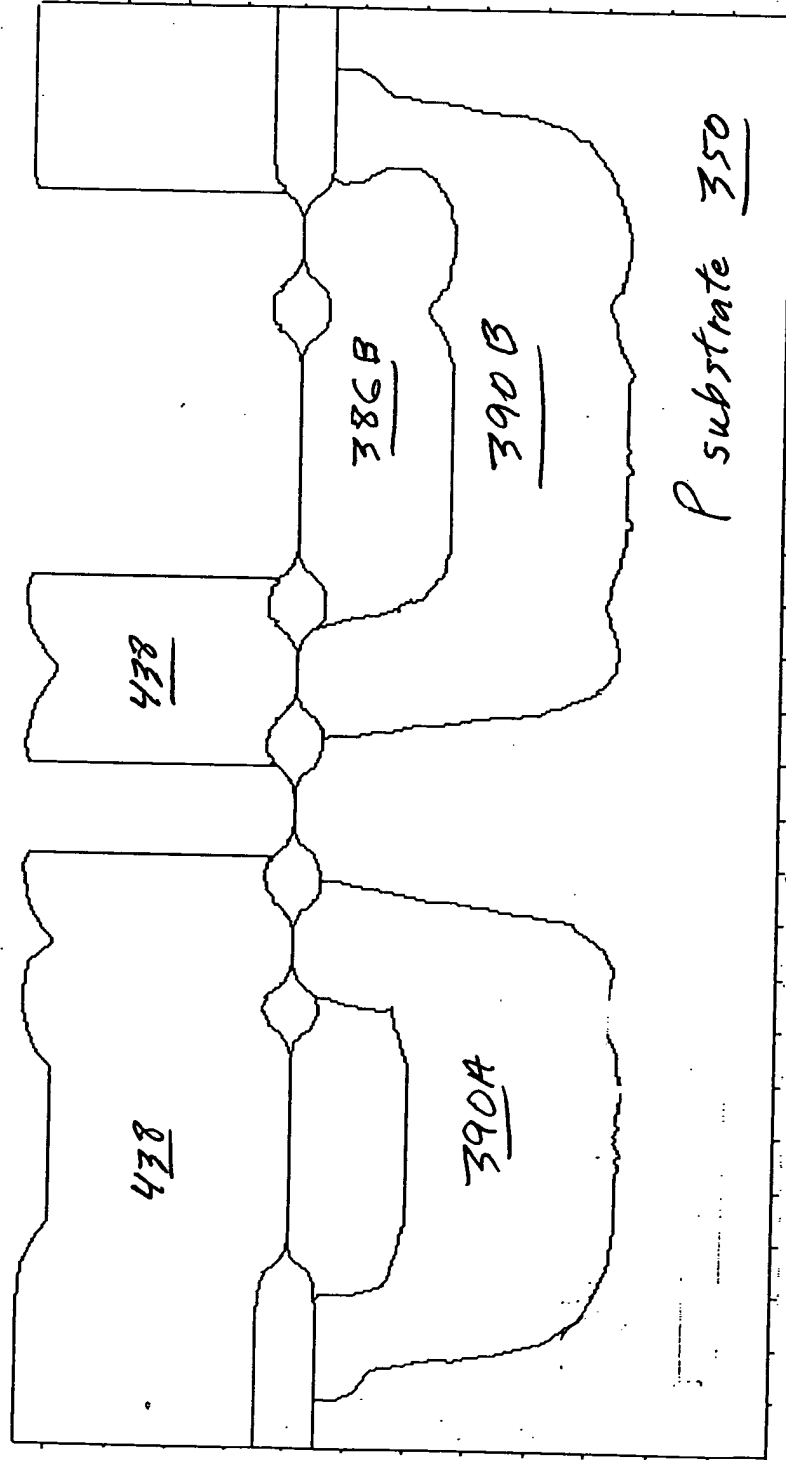
5V PNP 306



12V P Well Implant - First Stage

Fig. 43B

Conventional Layout
5V NPN 5V PNP

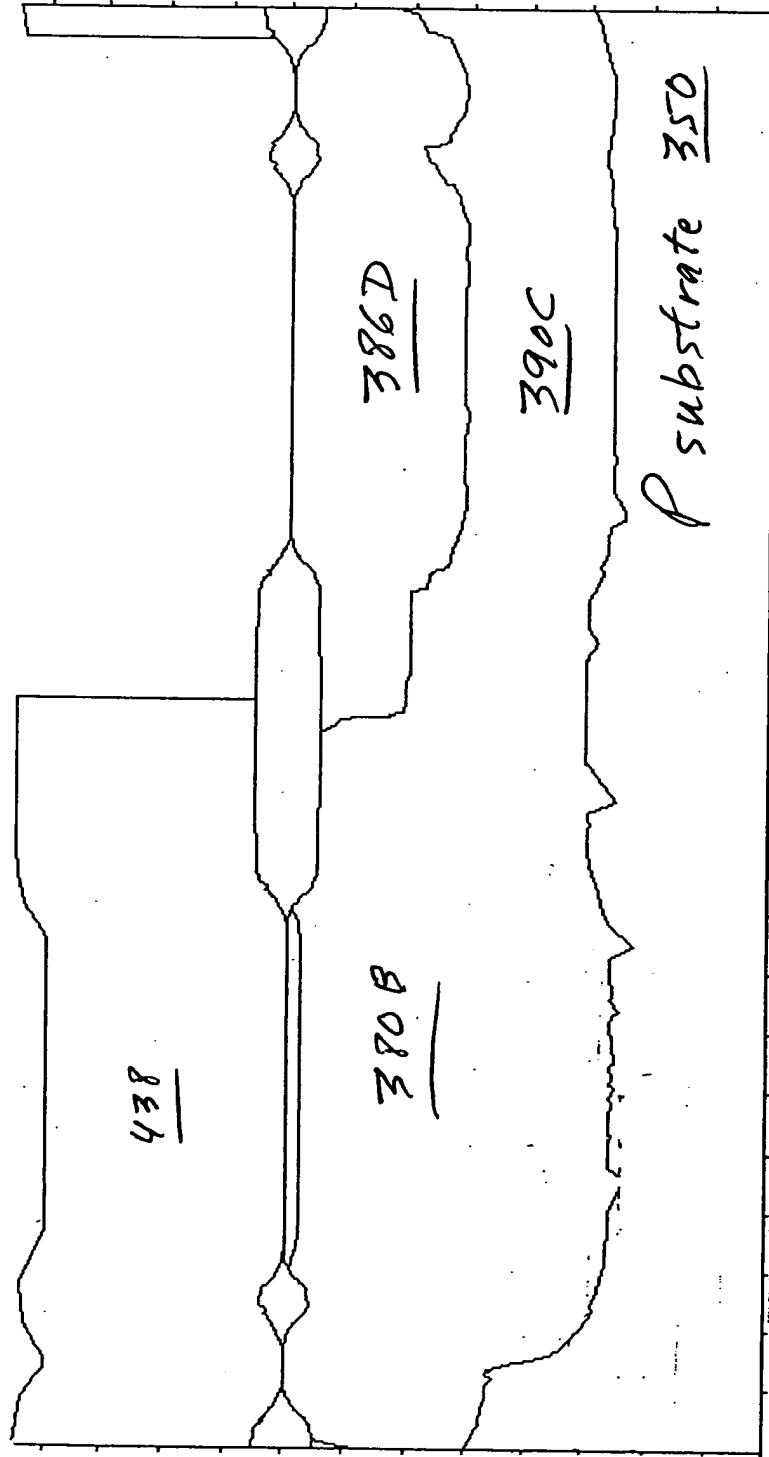


12V P Well Implant - First Stage
Fig. 43C

Symmetrical 12V CMOS

12V PMOS 309

12V NMOS 310



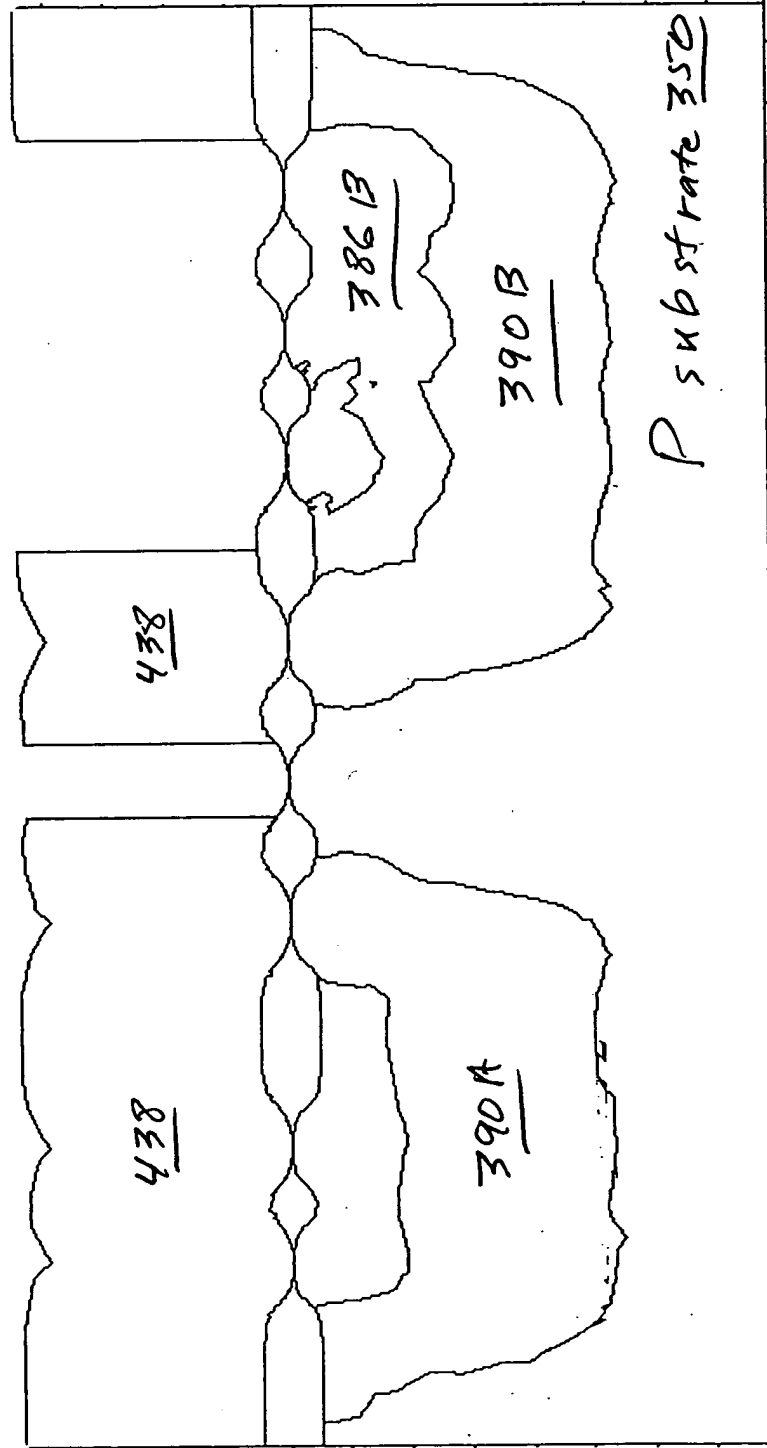
P substrate 350

12V PWell Implant - First Stage
Fig 43E

High F_T Layout

5V NPN 305

5V PNP 306



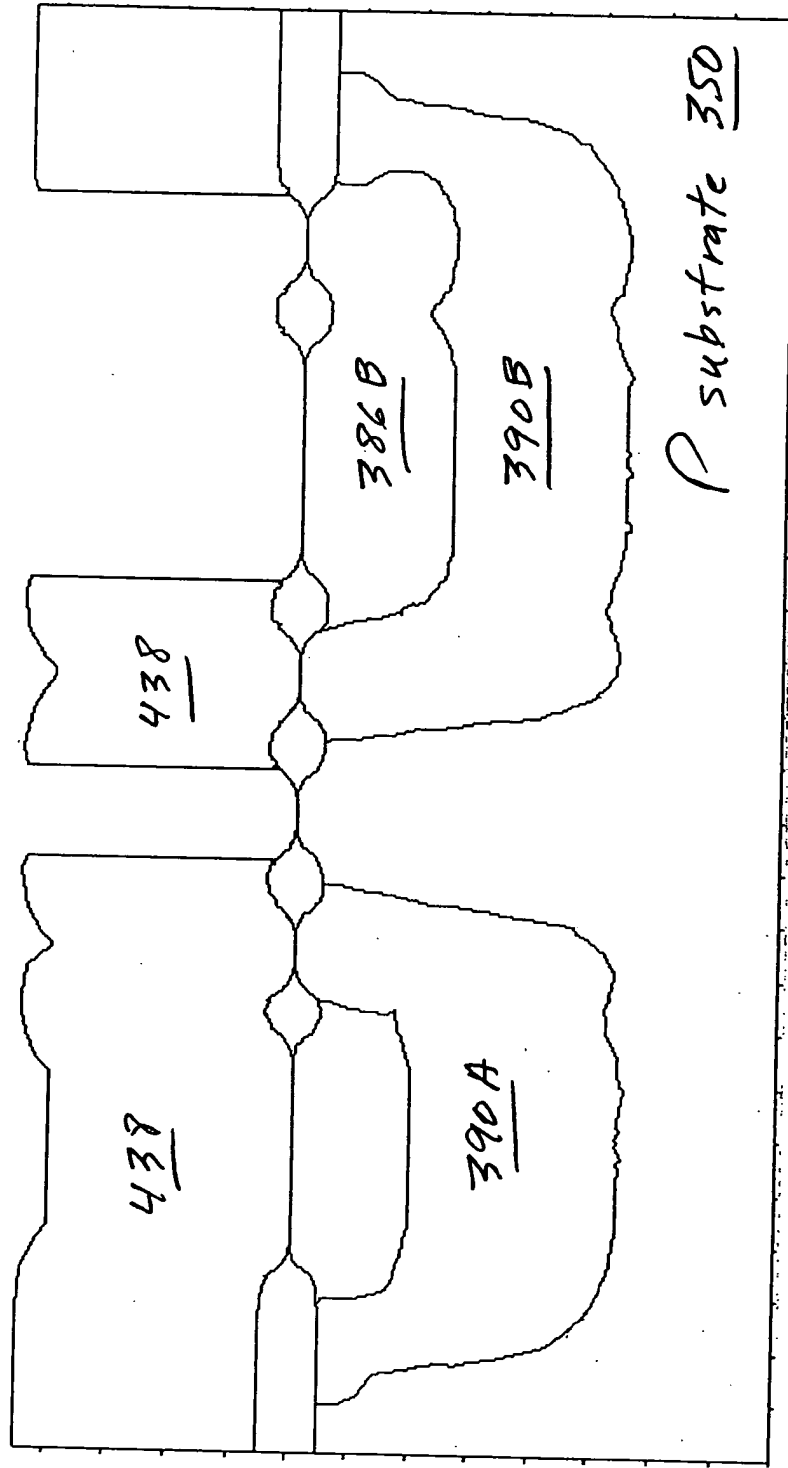
12V P Well Implant - Second Stage
Fig. 44B

140/219

Conventional Layout

5V NPN 305

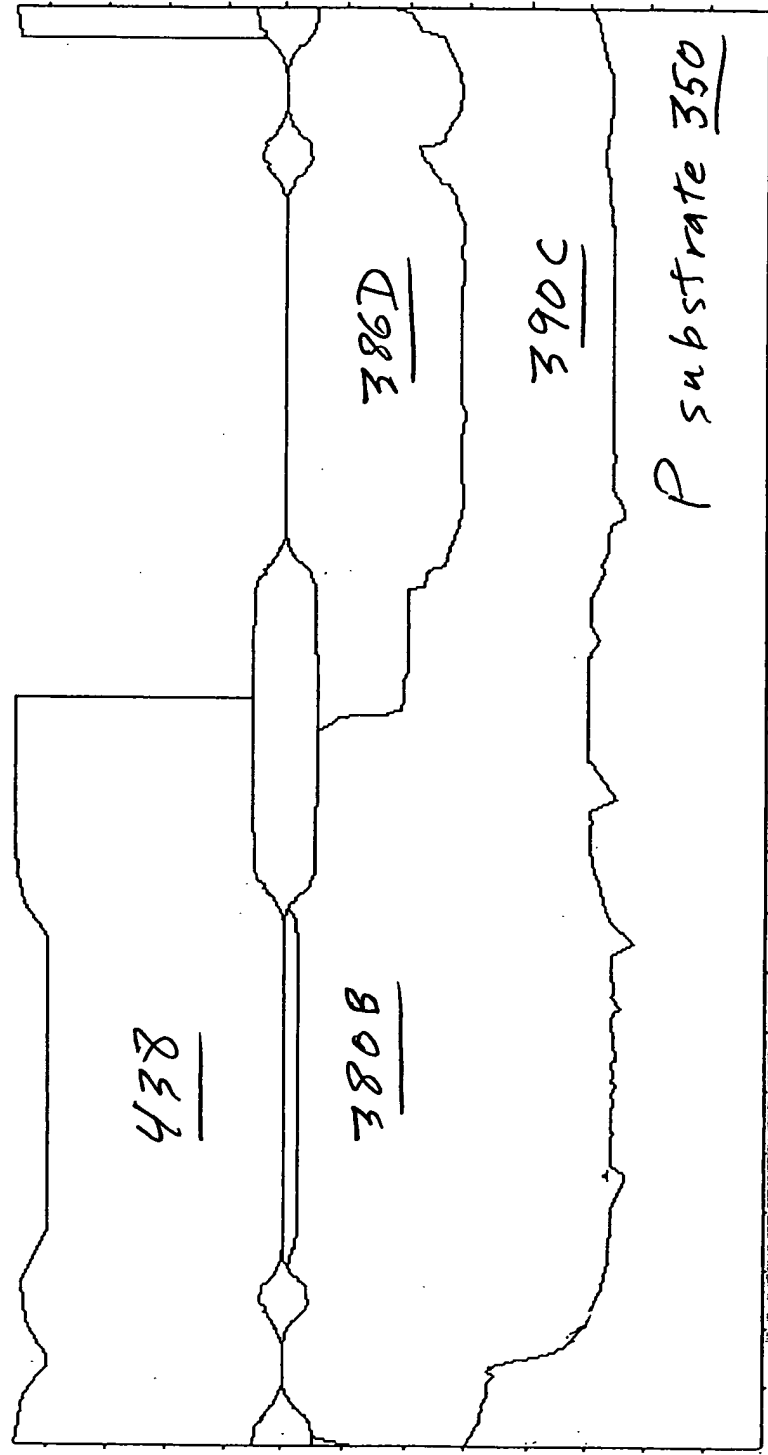
5V PNP 306



12V P Well Implant - Second Stage

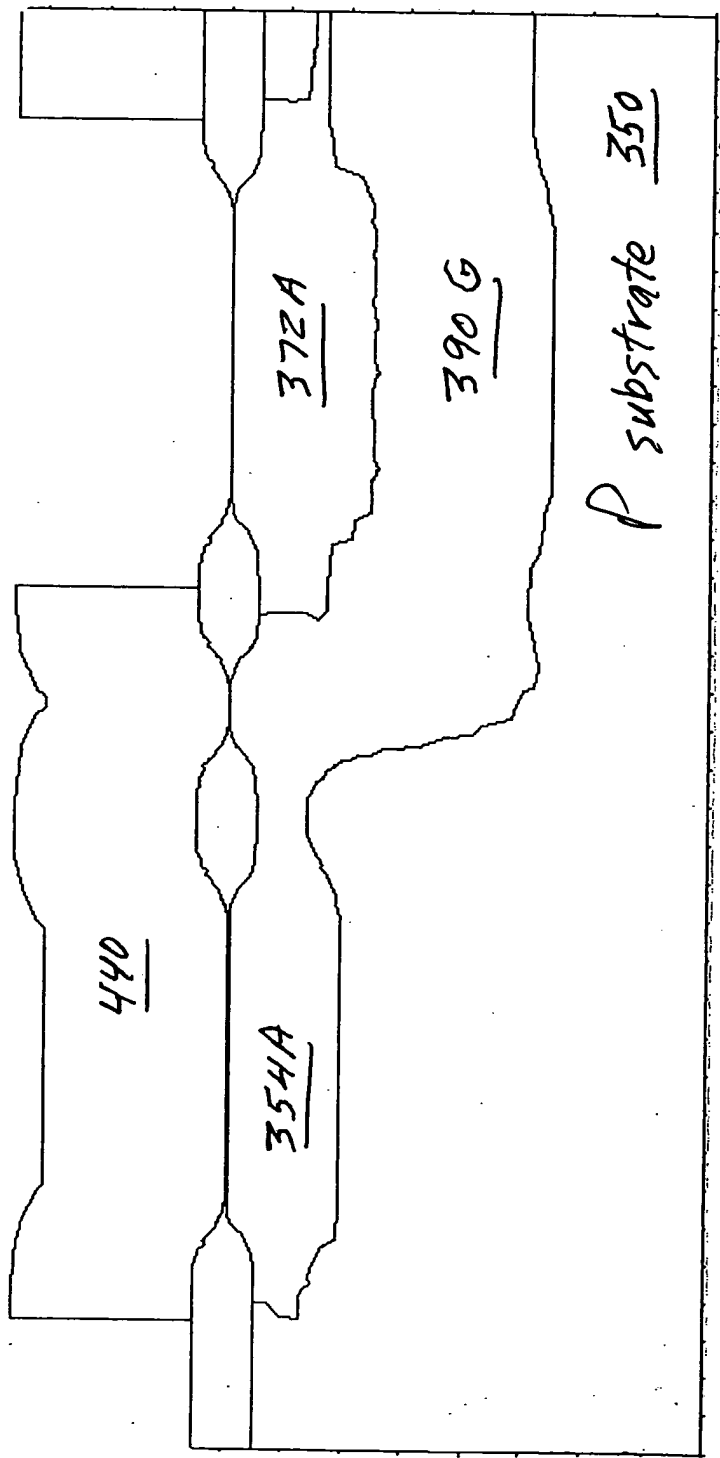
Fig 44C

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



12 V P Well Implant - Second Stage
Fig. 44E

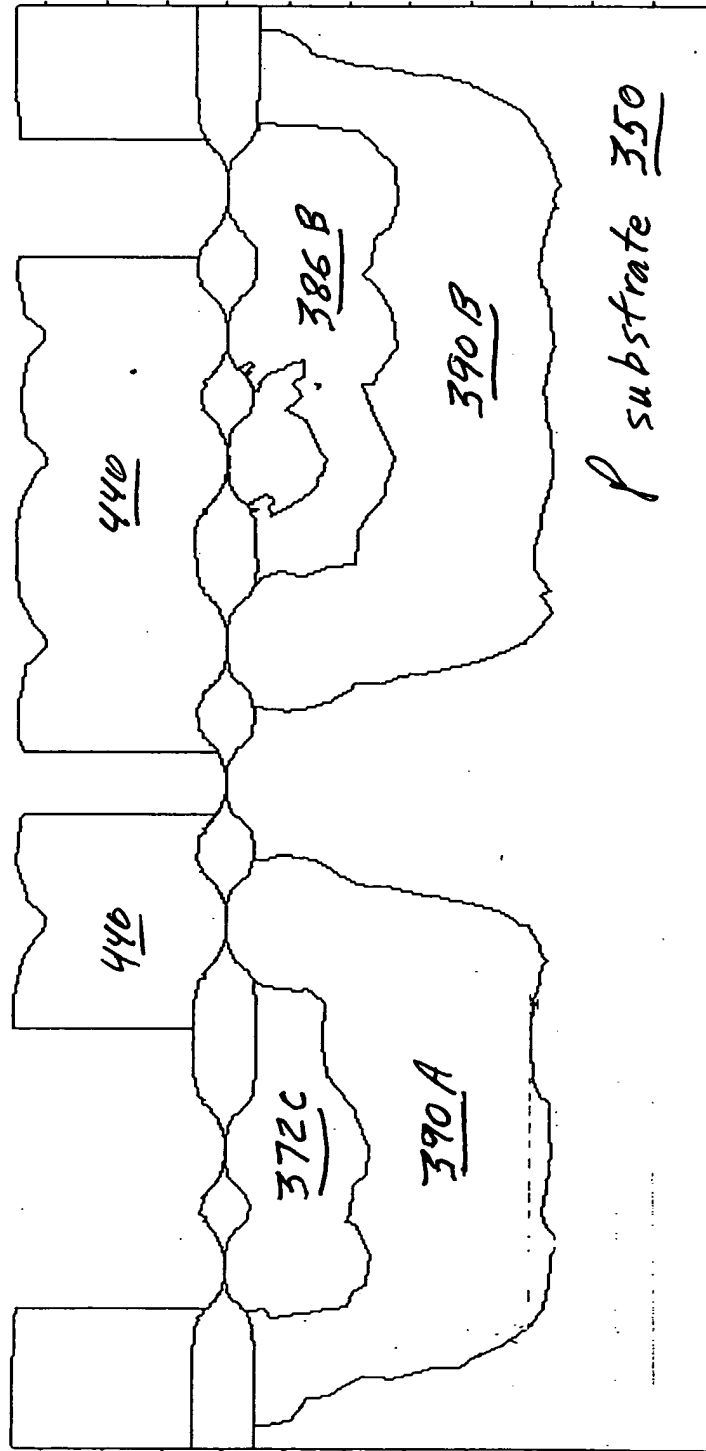
5V PMOS 301 5V NMOS 302



5V P Well Implant - First Stage
Fig. 45A

High F_T Layout

5V NPN 305 5V PNP 306



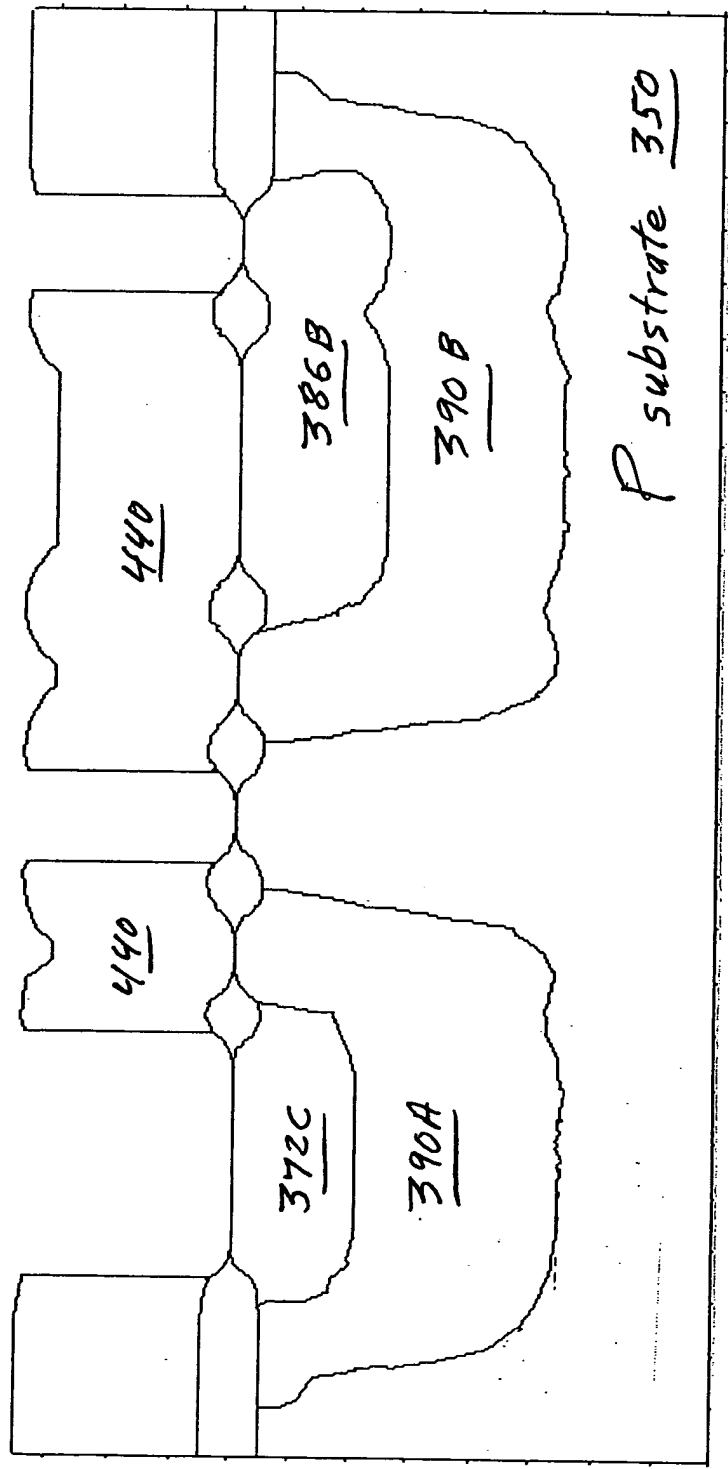
5V P Well Implant - First Stage

Fig. 45B

Conventional Layout

5V NPN

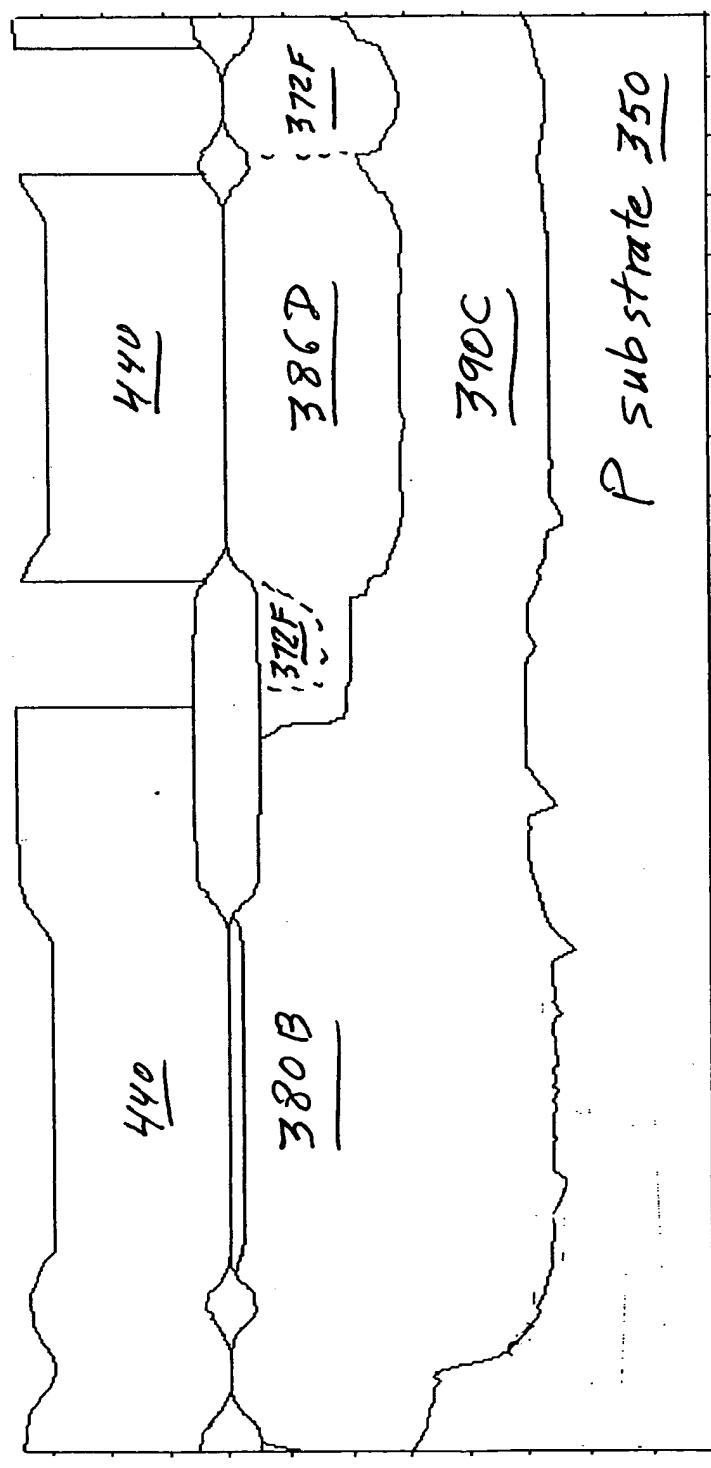
5V PNP



5V P Well Implant - First Stage

Fig. 45C

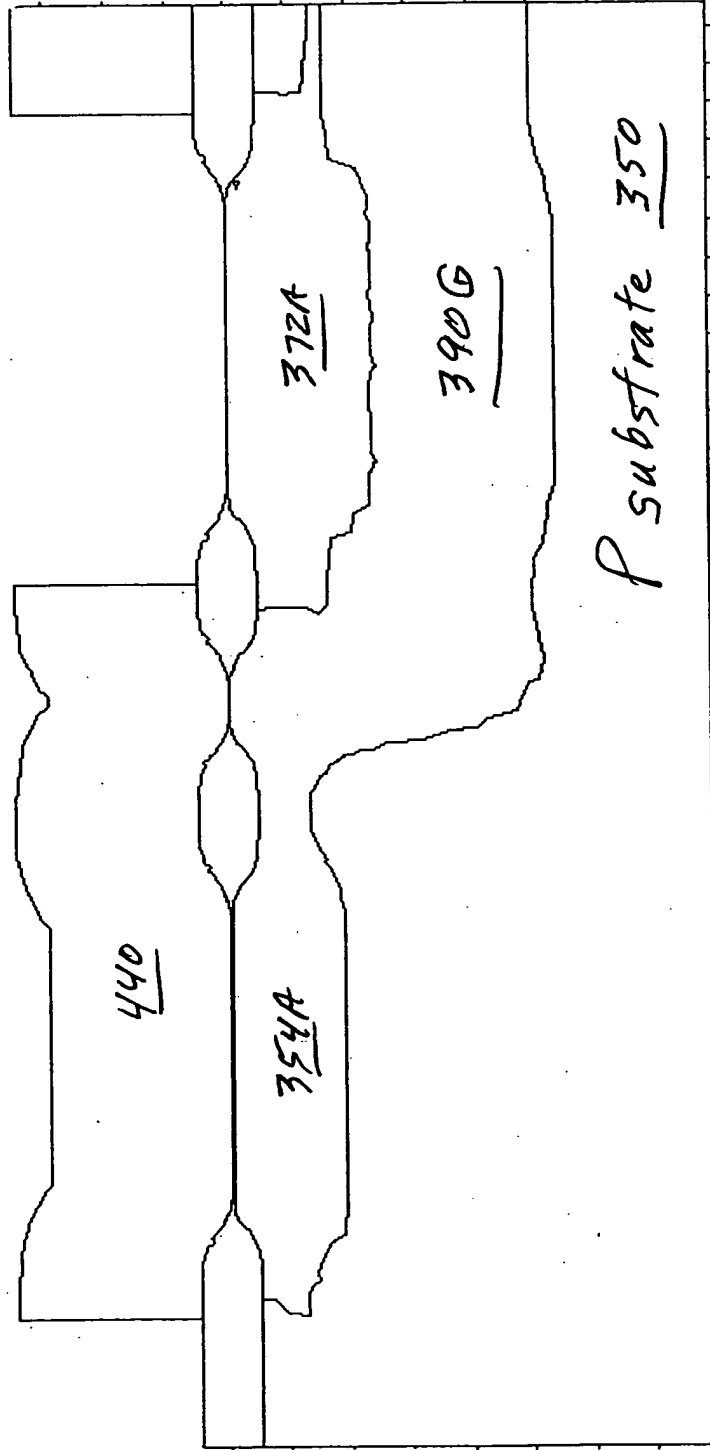
Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



5V P Well Implant - First Stage
Fig. 45E

146/219

5V PMOS 301 5V NMOS 302

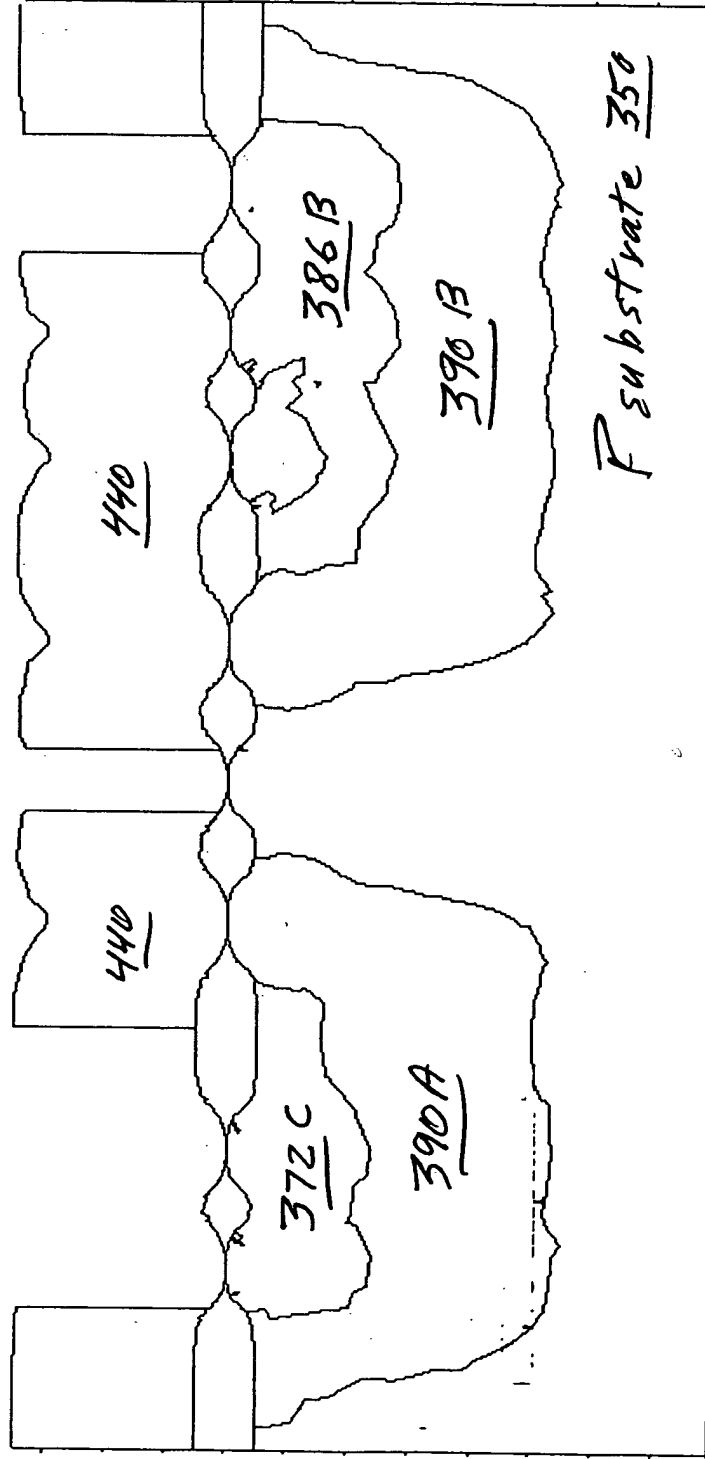


5V P Well Implant - Second Stage
Fig 46A

High F_T Layout

5V NPN 305

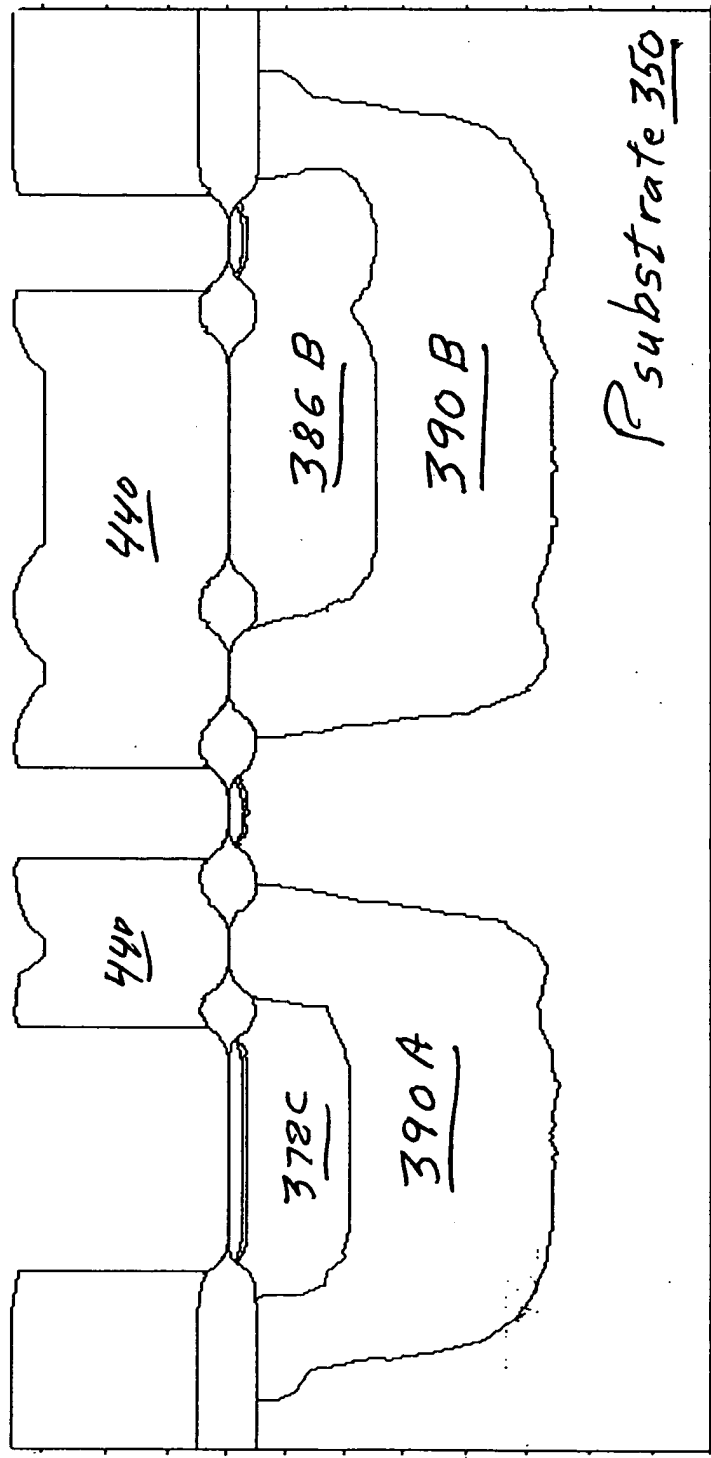
5V PNP 306



5V P Well Implant - Second Stage

Fig. 46B

Conventional Layout
5V NPN 305 5V PNP 306

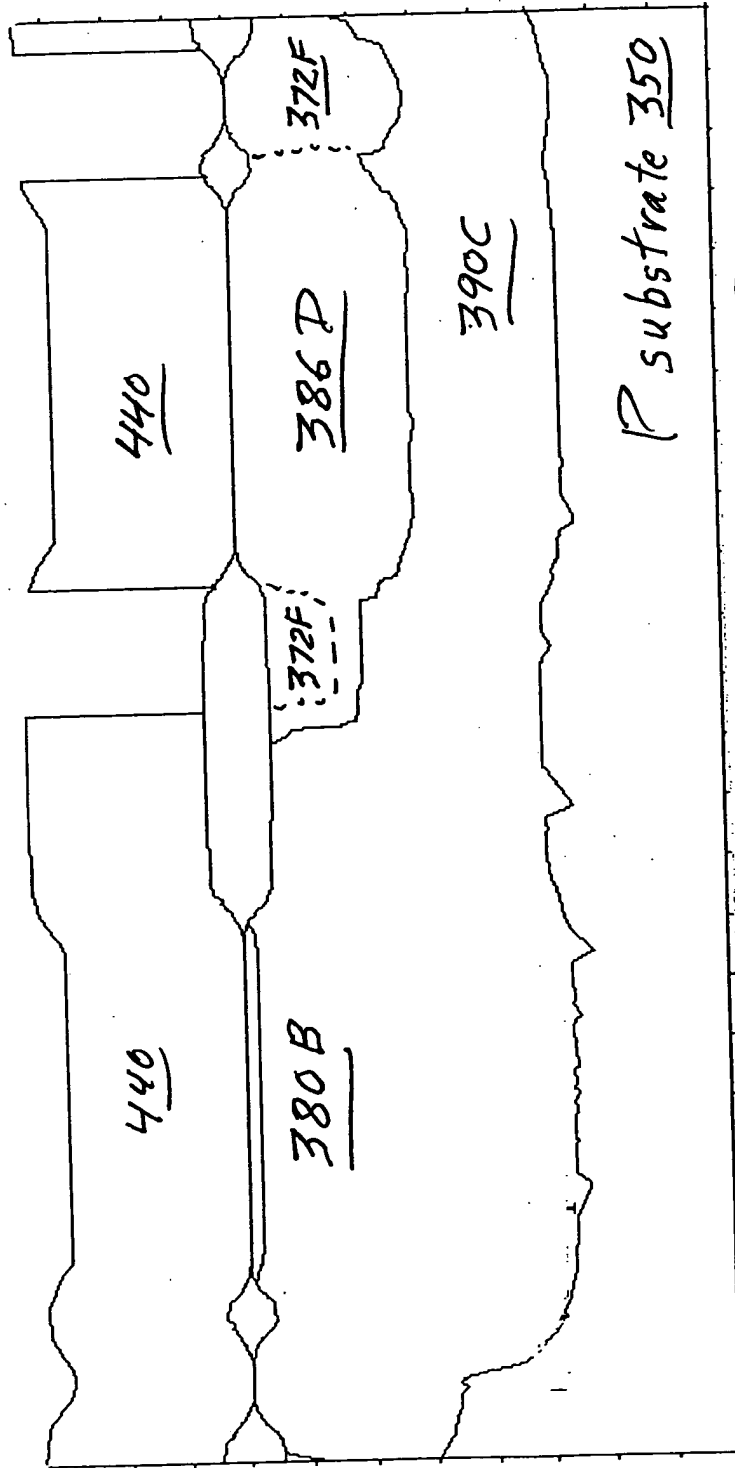


5V P Well Implant - Second Stage

Fig. 46C

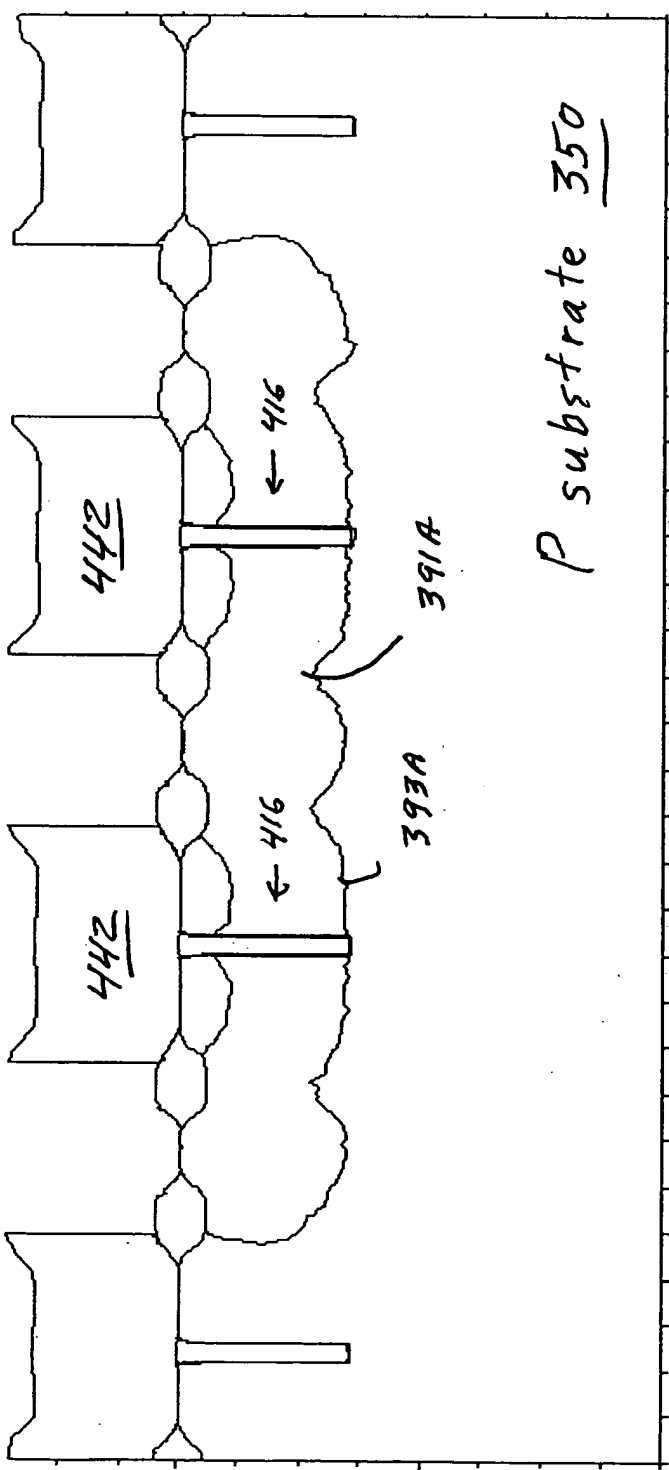
149/219

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



5V P Well Implant - Second Stage
Fig. 46E

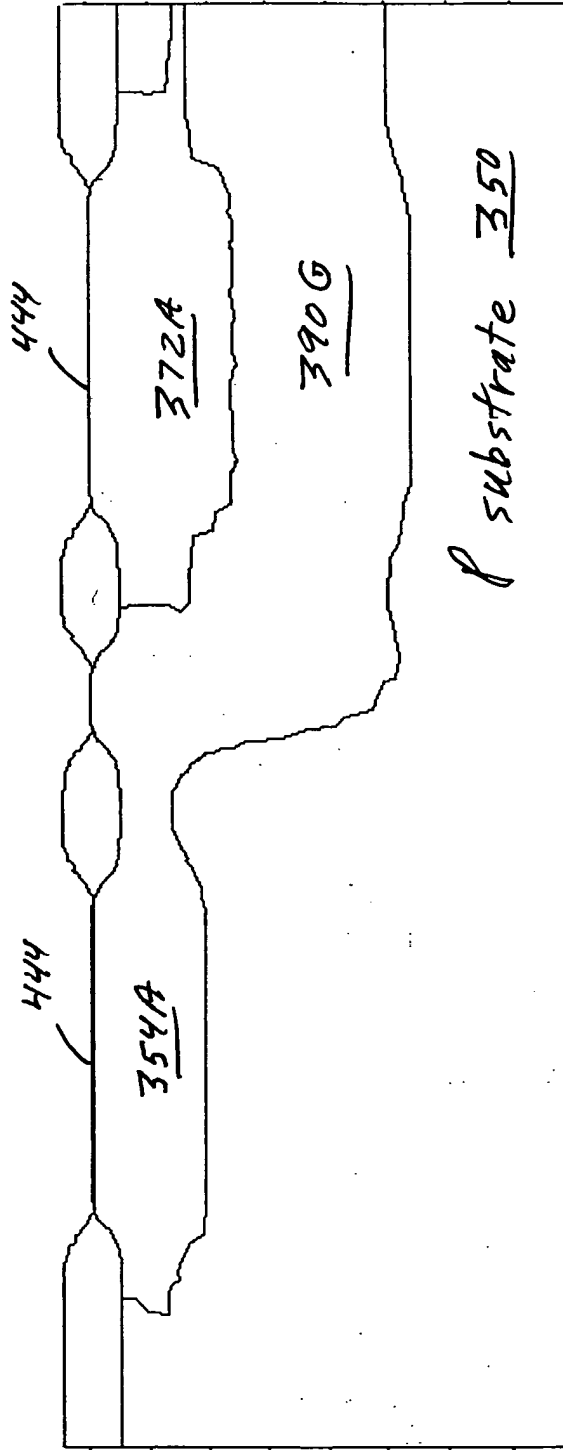
30V Lateral Trench Dmos 308



Etch-Block Mask and Etching of Planar Active Regions
Fig 47D

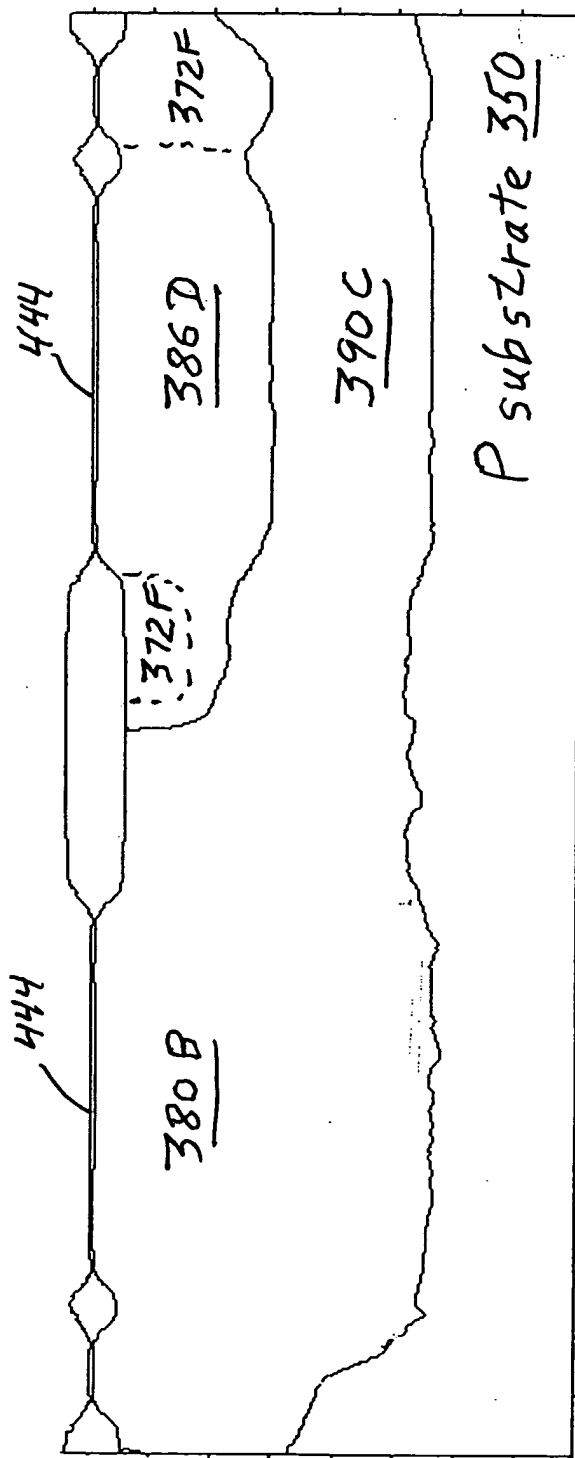
151/219

5V PMOS 301 5V NMOS 302



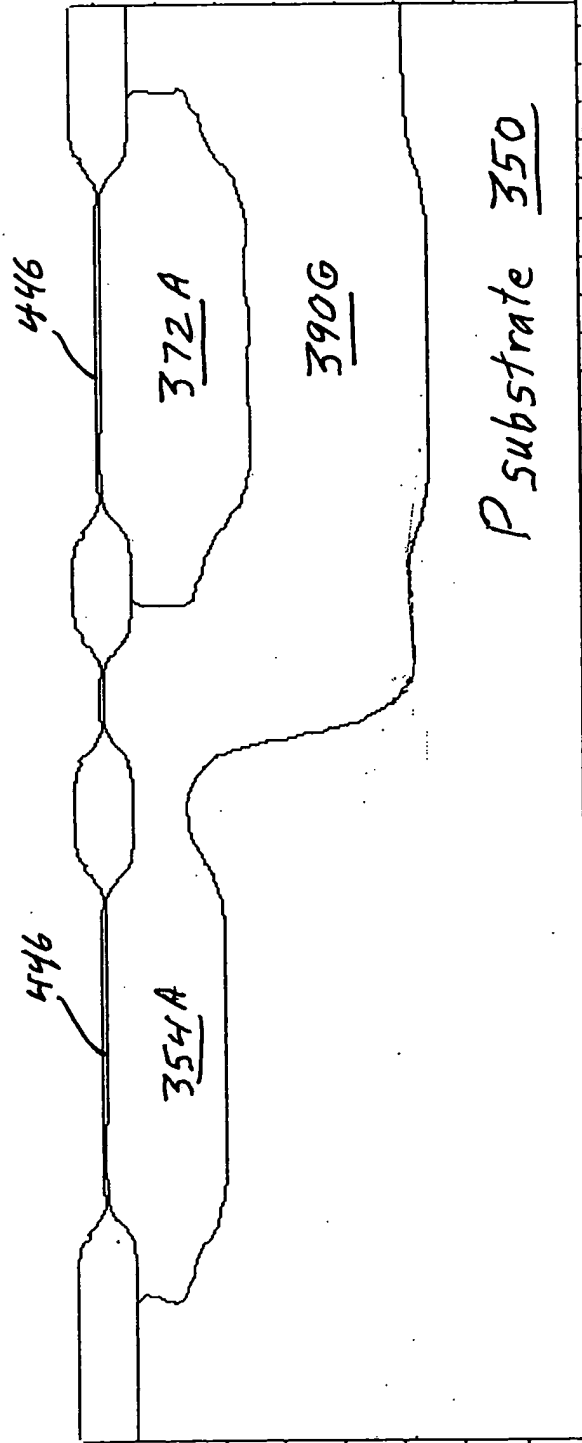
First Planar Gate Oxide
Fig. 42A

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



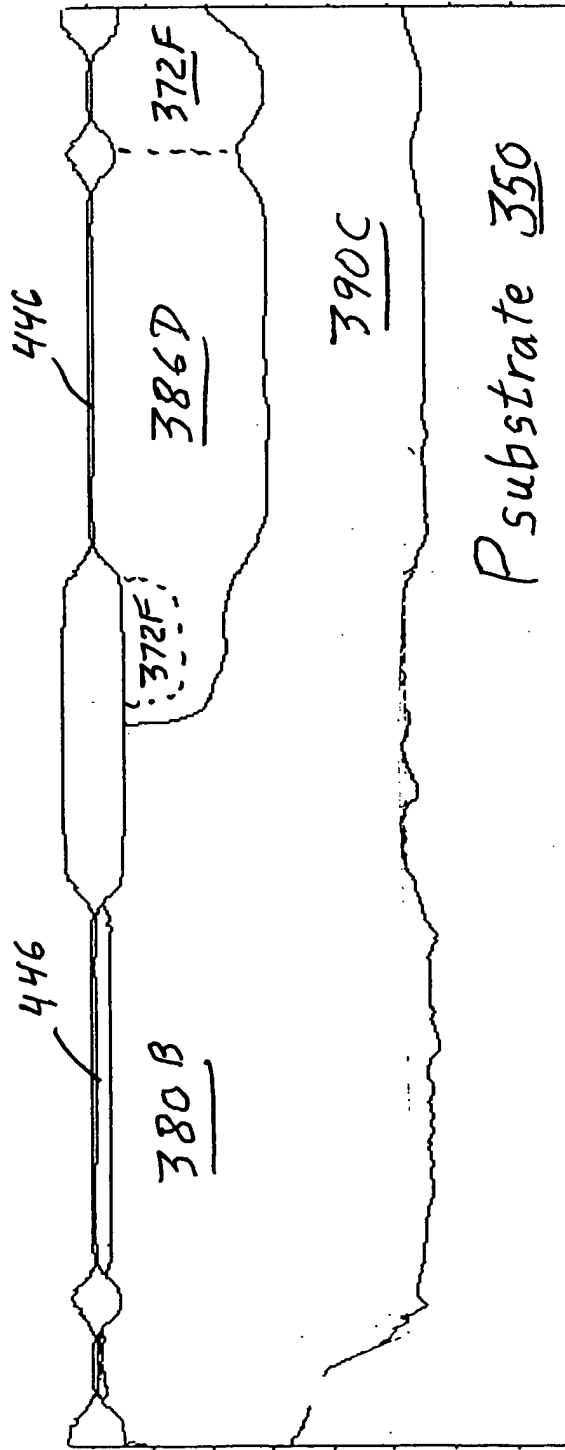
First Planar Gate Oxide
Fig 48E

5V PMOS 301 5V NMOS 302



Threshold Adjust Implant - First Stage
Fig. 49A

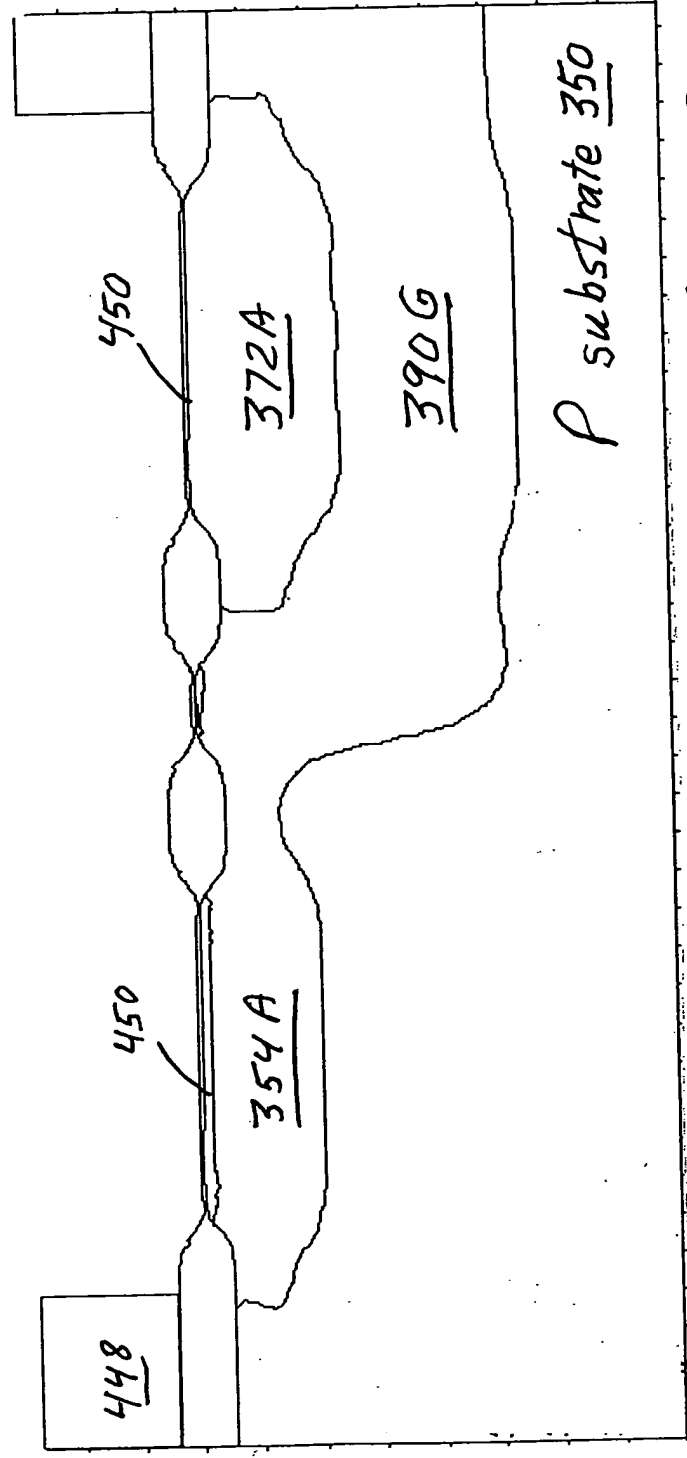
Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



Threshold Adjust Implant - First Stage
Fig. 49E

5V NMOS 302

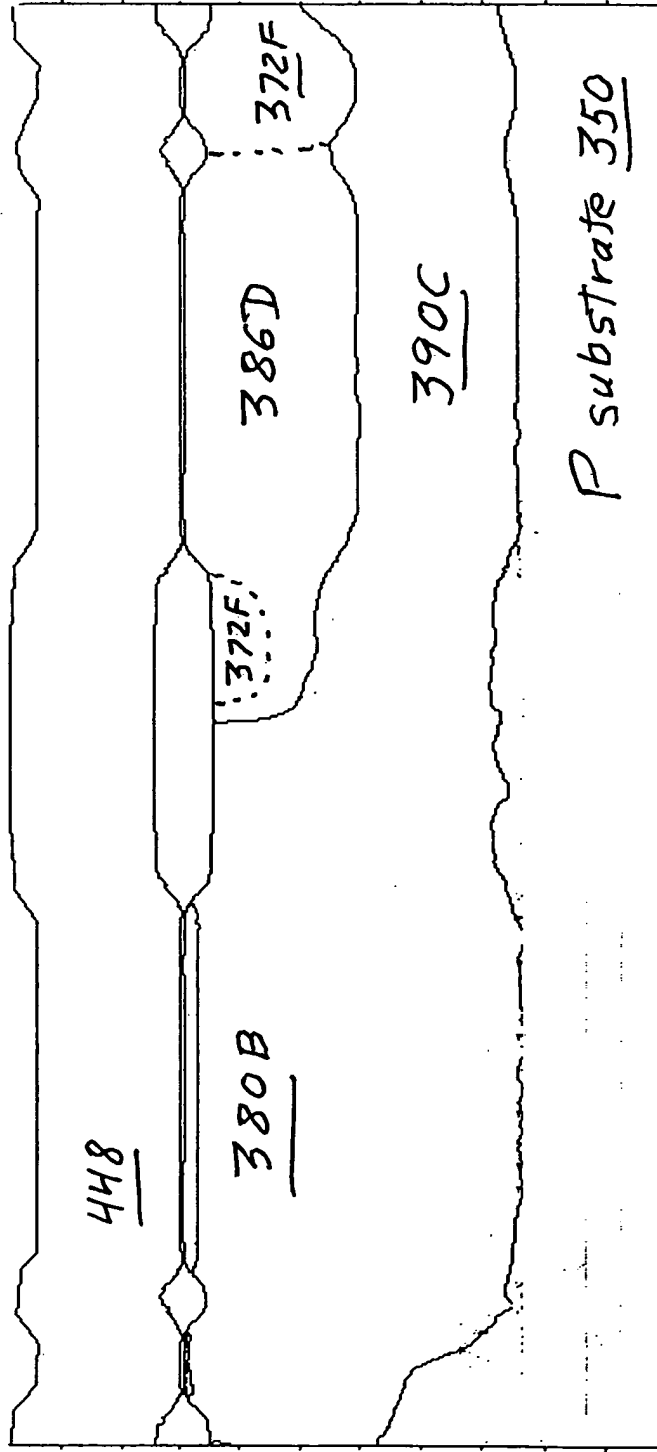
5V PMOS 301



Threshold Adjust Implant - Second Stage
First Planar Gate Oxide Removal

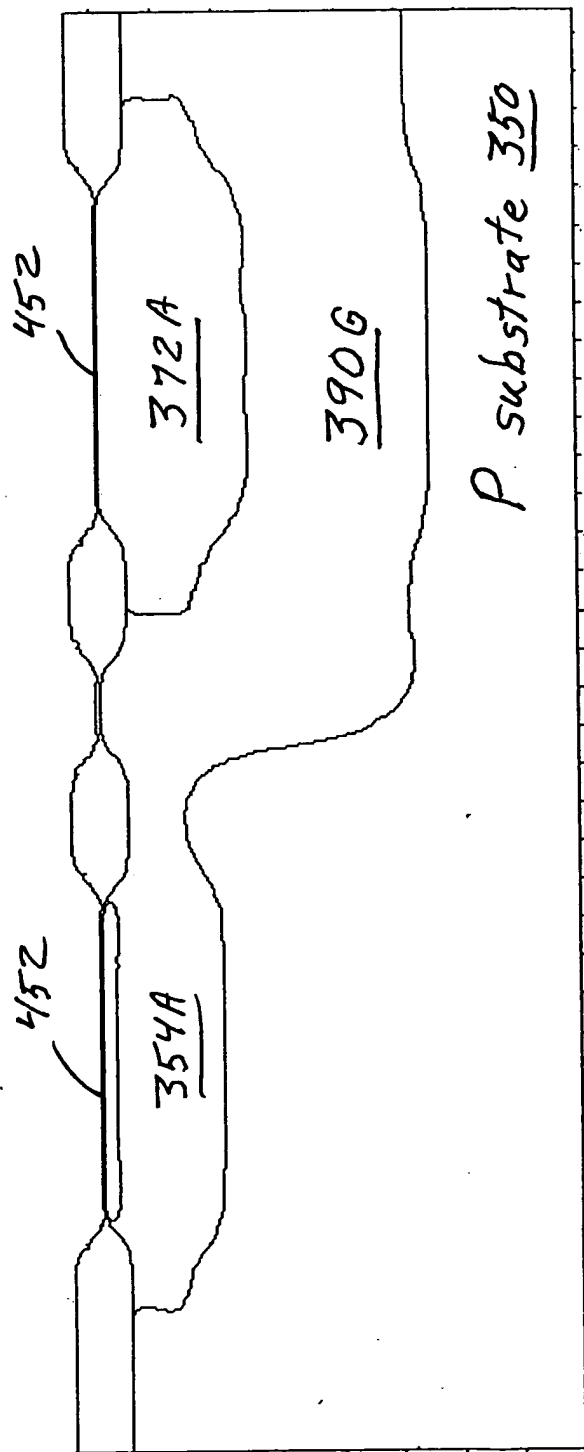
Fig. 50A

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



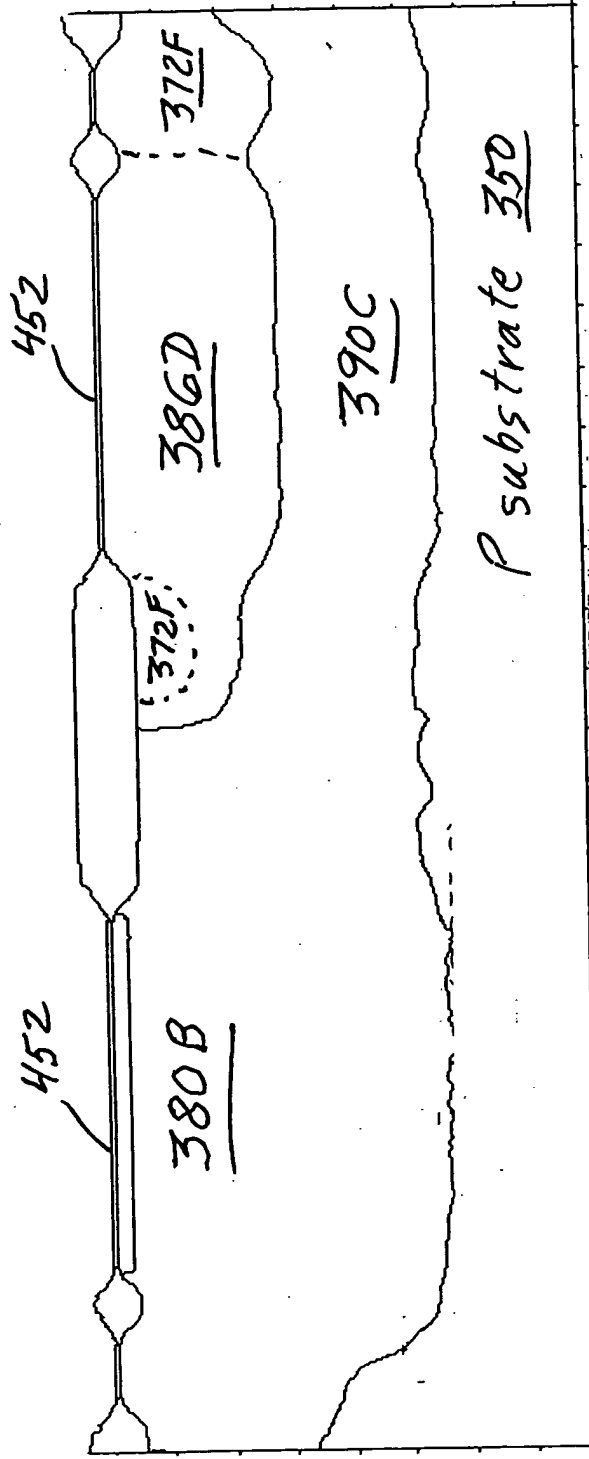
Threshold Adjust Implant - Second Stage
Fig. 50E

5V PMOS 301 5V NMOS 302



Second Planar Gate Oxide
Fig. 51A

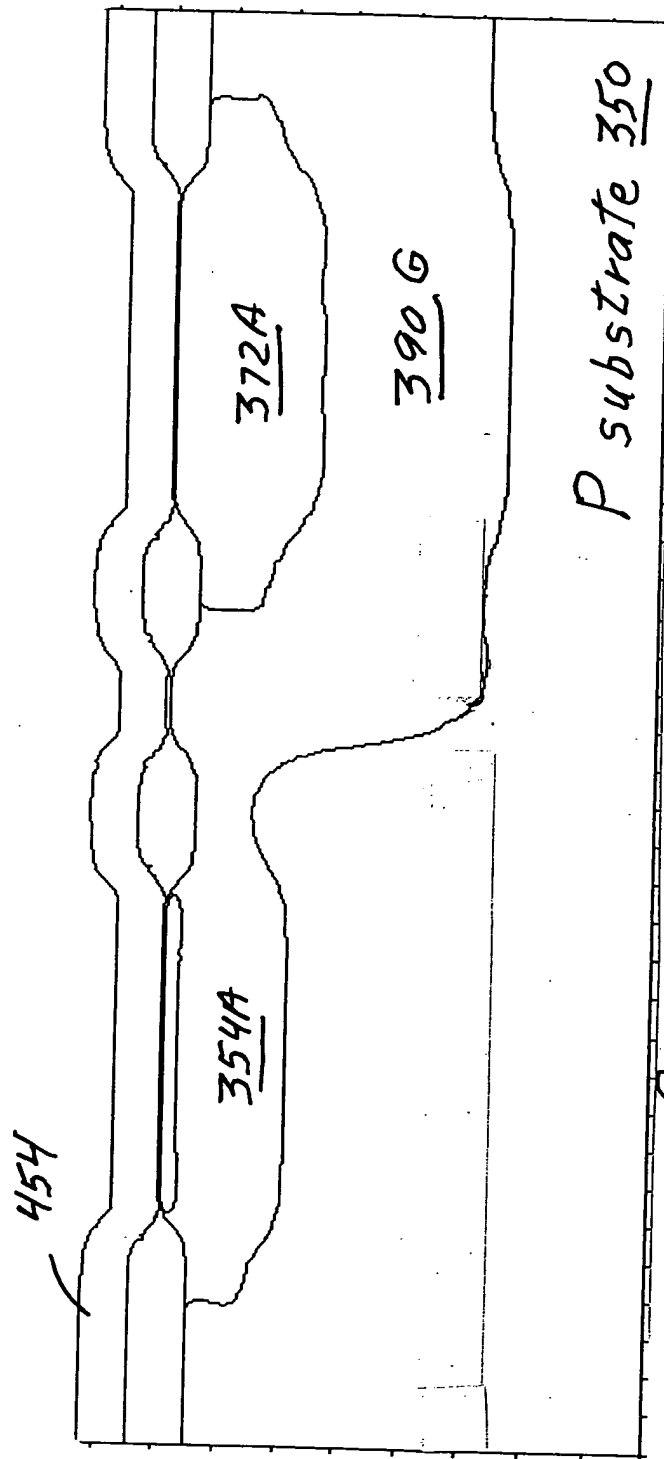
Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



Second Planar Gate Oxide

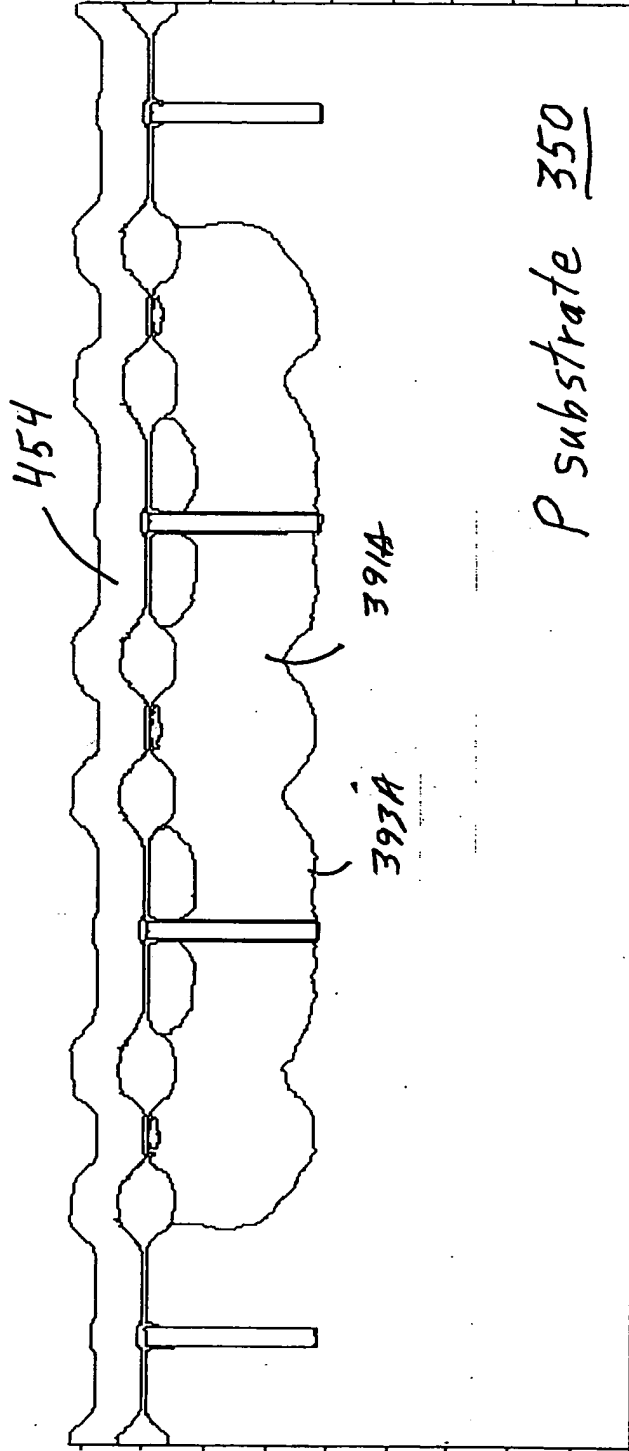
Fig. 51E

5V PMOS 301 5V NMOS 302



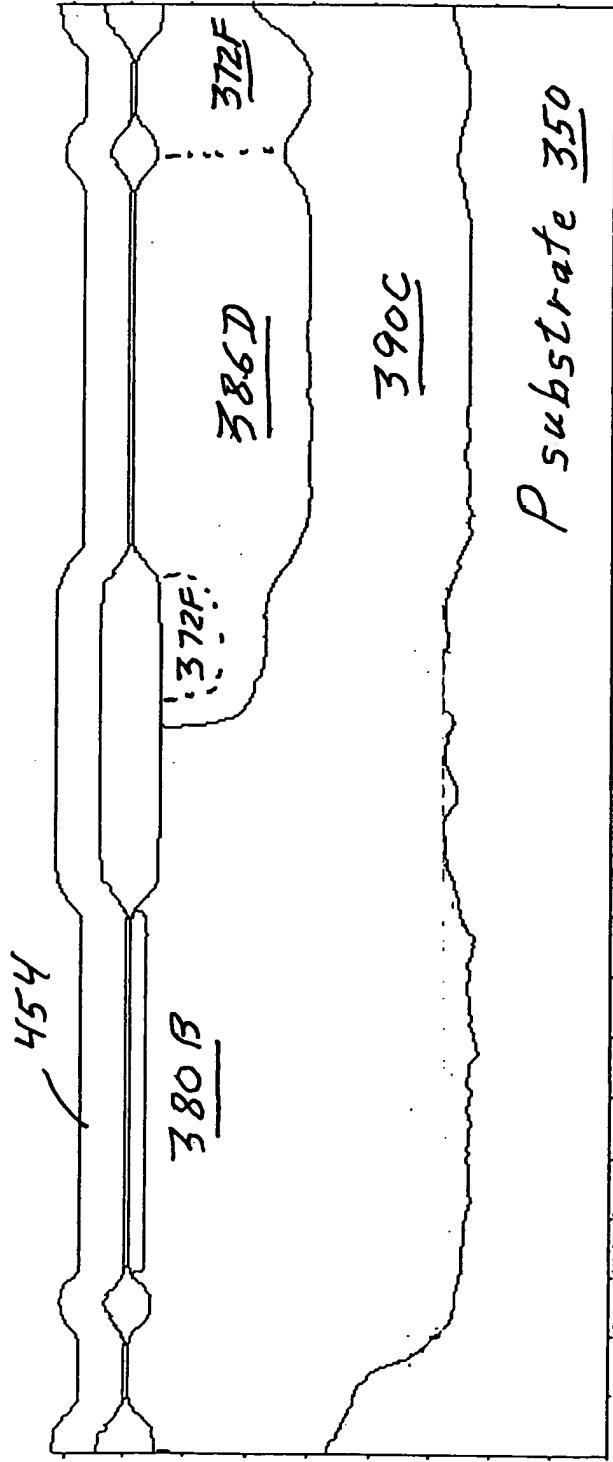
Polysilicon - Third Layer
Fig. 52A

30V Lateral Trench DMOS 308



Polysilicon - Third Layer
Fig. 52D

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310

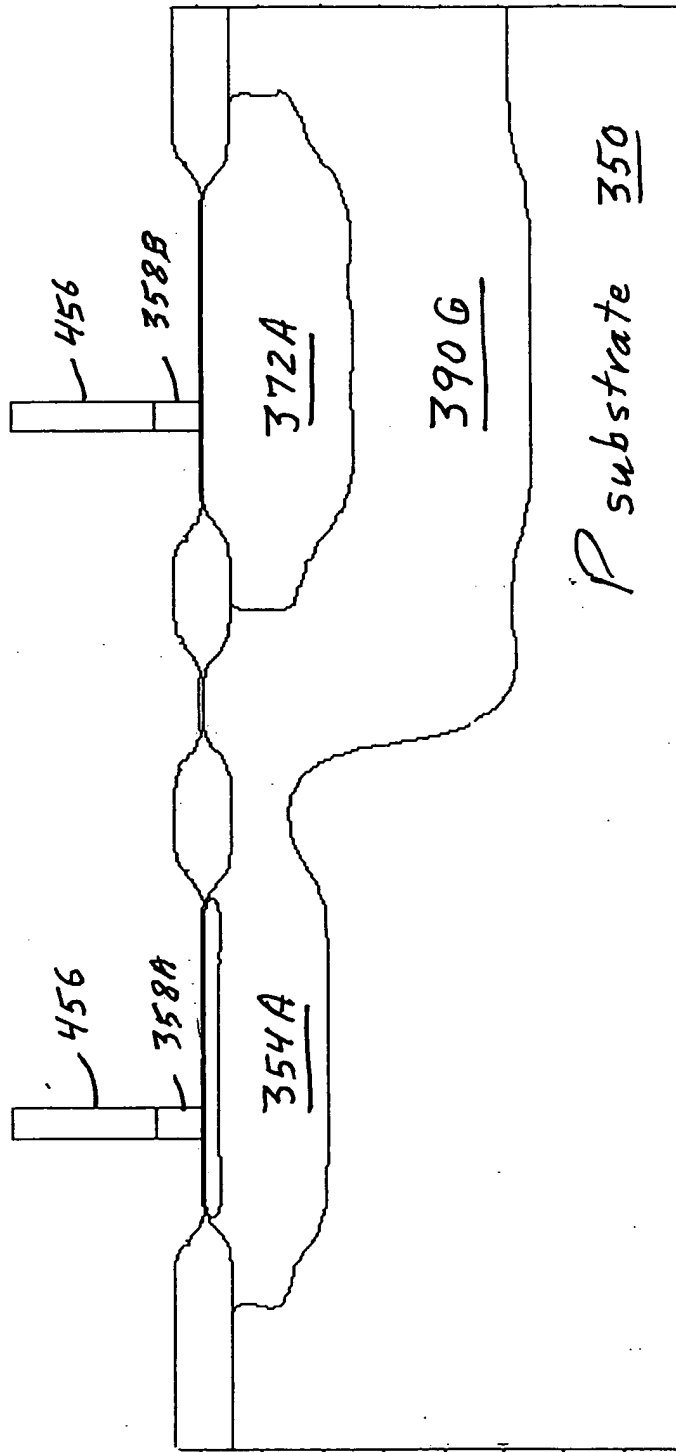


Polysilicon - Third Layer
Fig. 52 E

161/219

5V PMOS 301

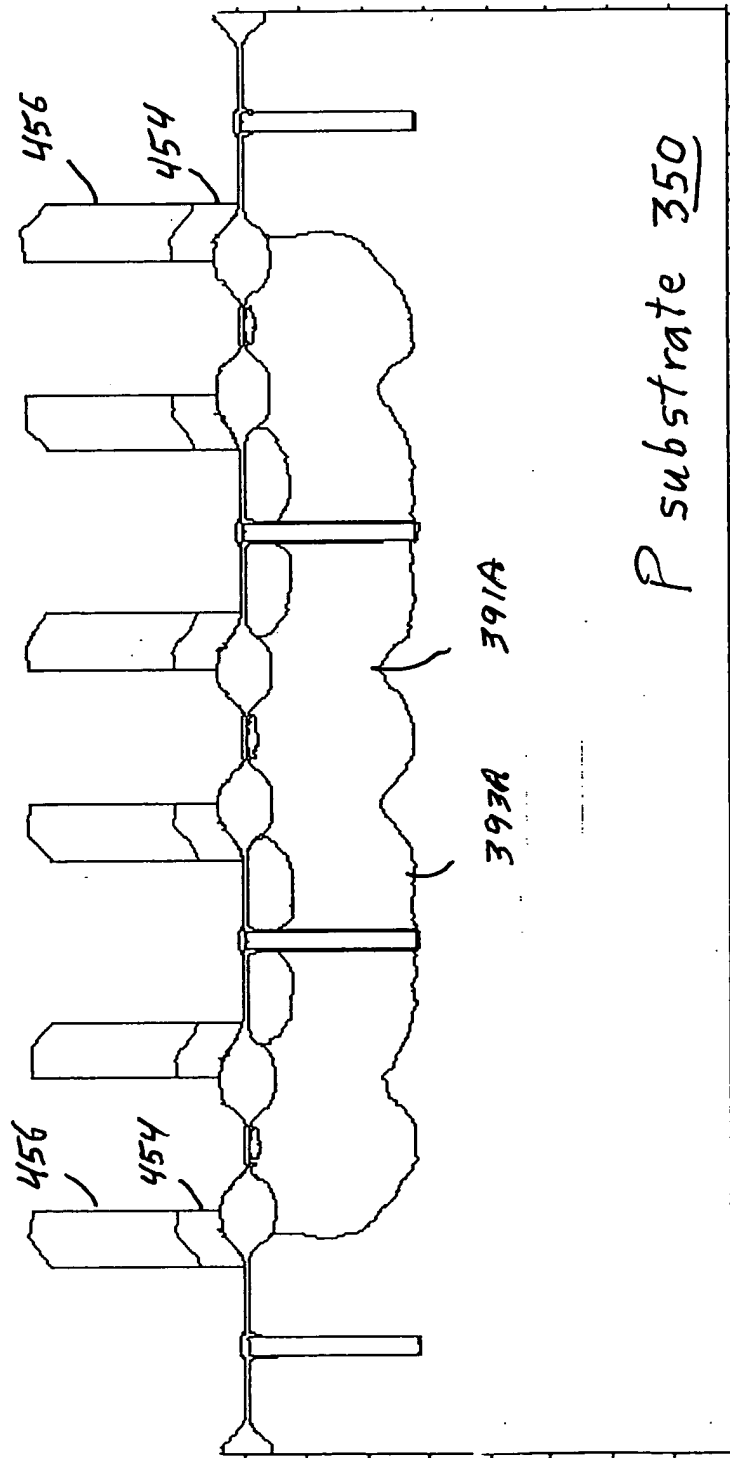
5V NMOS 302



Planar Gate Formation
Fig. 53A

163/219

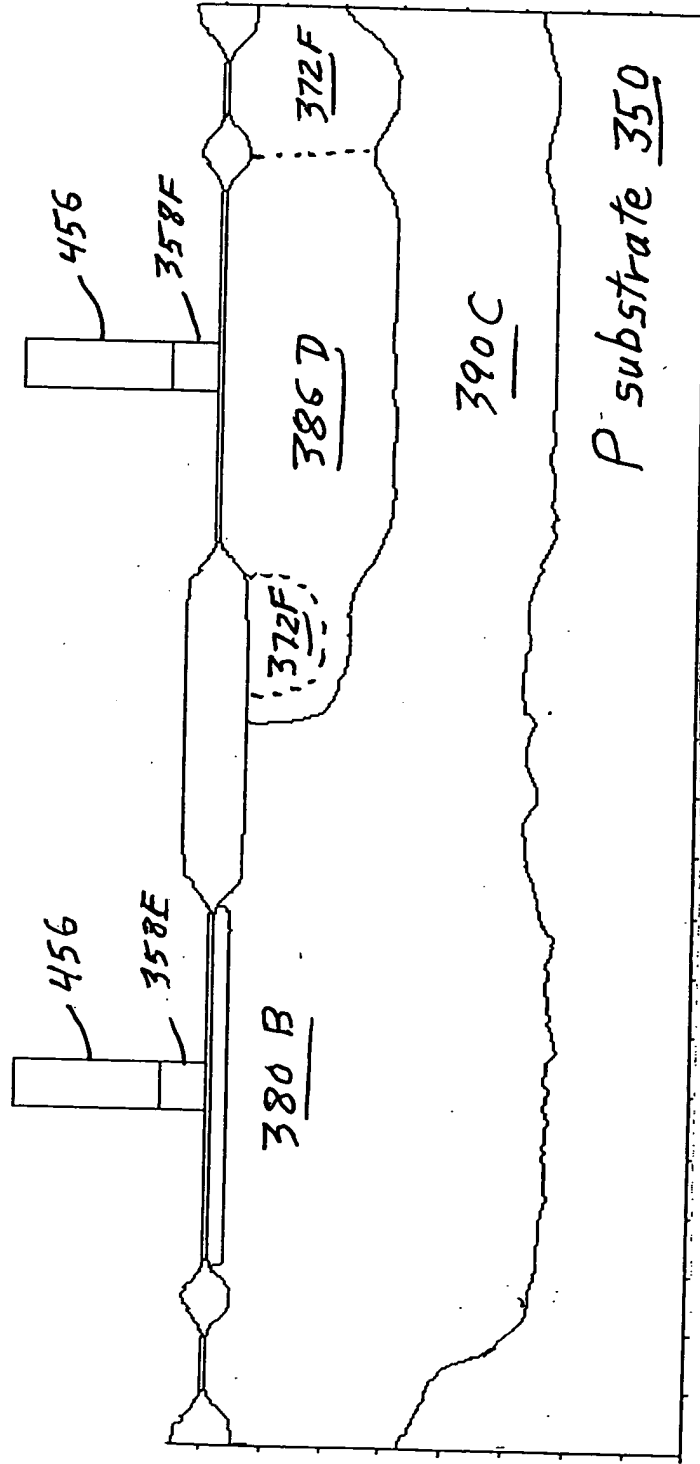
30V Lateral Trench DMOS 308



P substrate 350

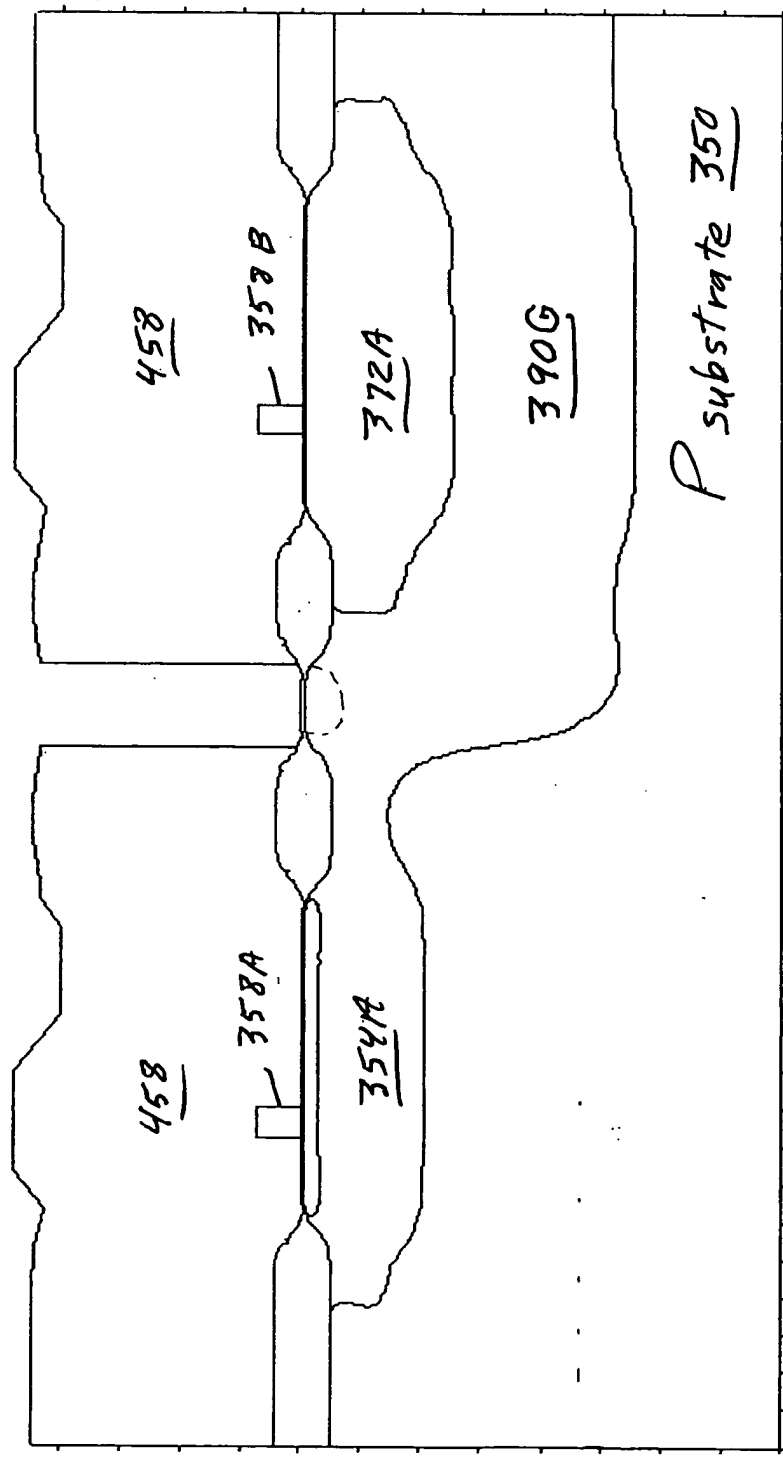
Fig. 53D Planar Gate Formation

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



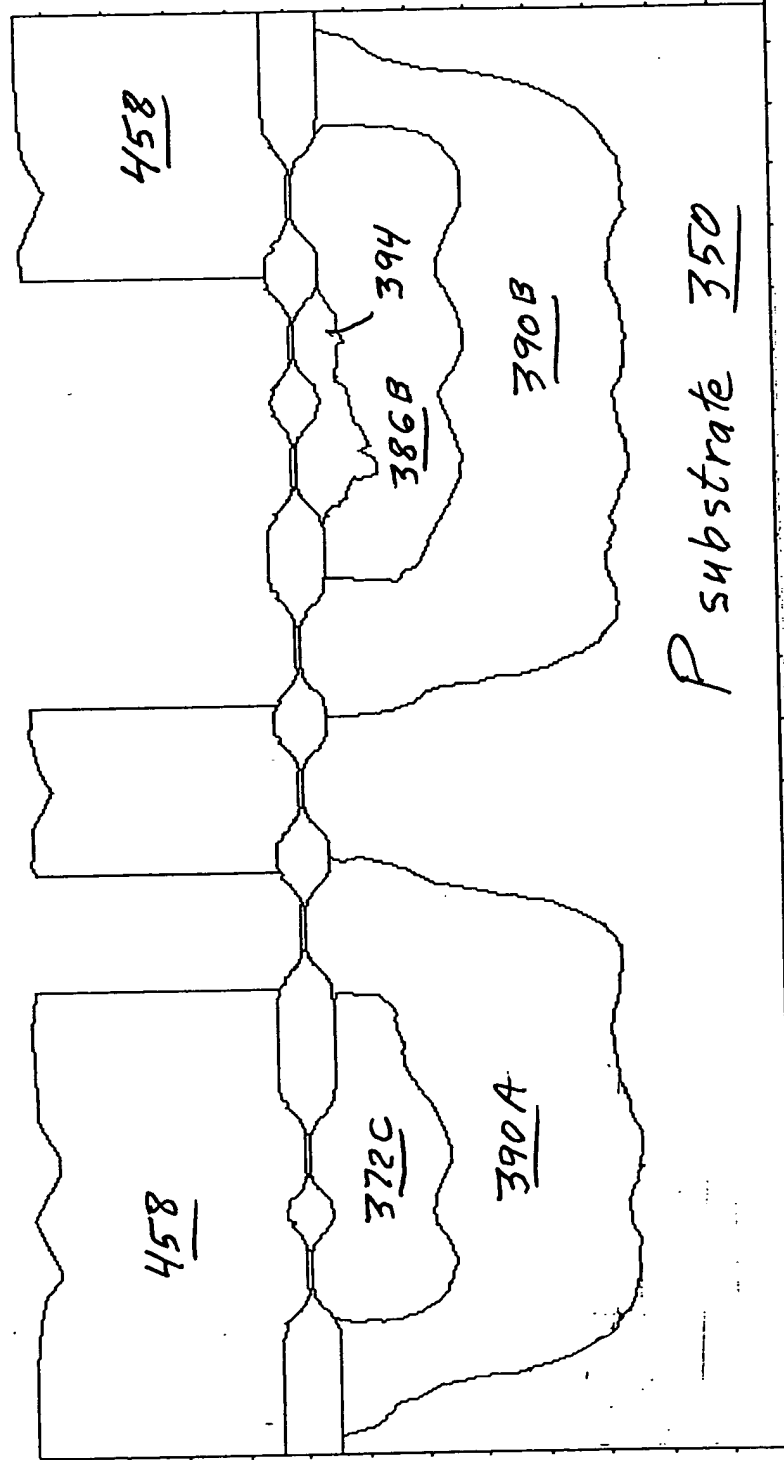
Planar Gate Formation
Fig 53E

5V PMOS 301 5V NMOS 302



N-Base Mask and Implant
Fig. 54A

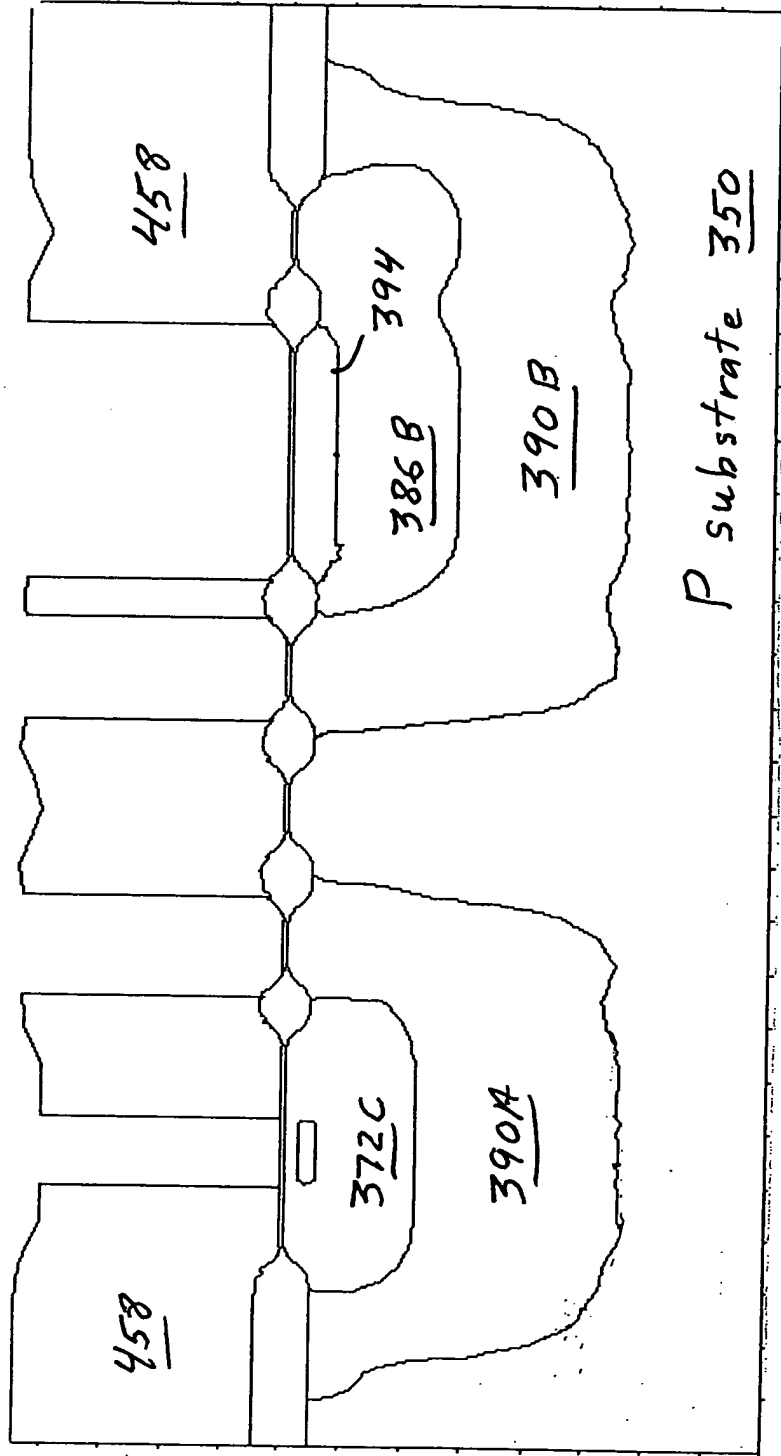
High F_T Layout
5V NPN 305 5V PNP 306



N-Base Mask and Implant

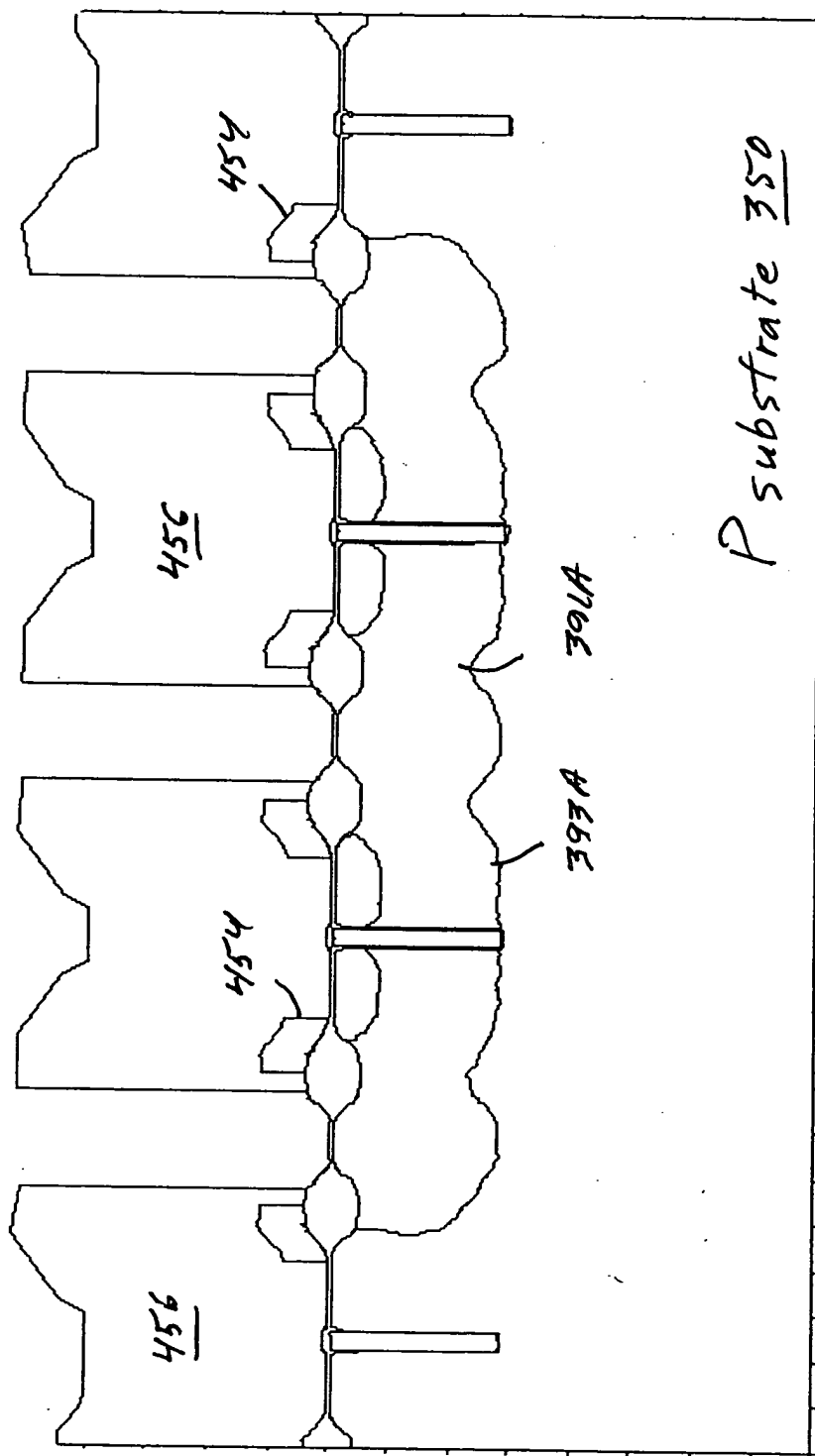
Fig. 54B

Conventional Layout
5V NPN 305 5V PNP 306



N-Base Mask and Implant
Fig. 54C

30V Lateral Trench DMS 308

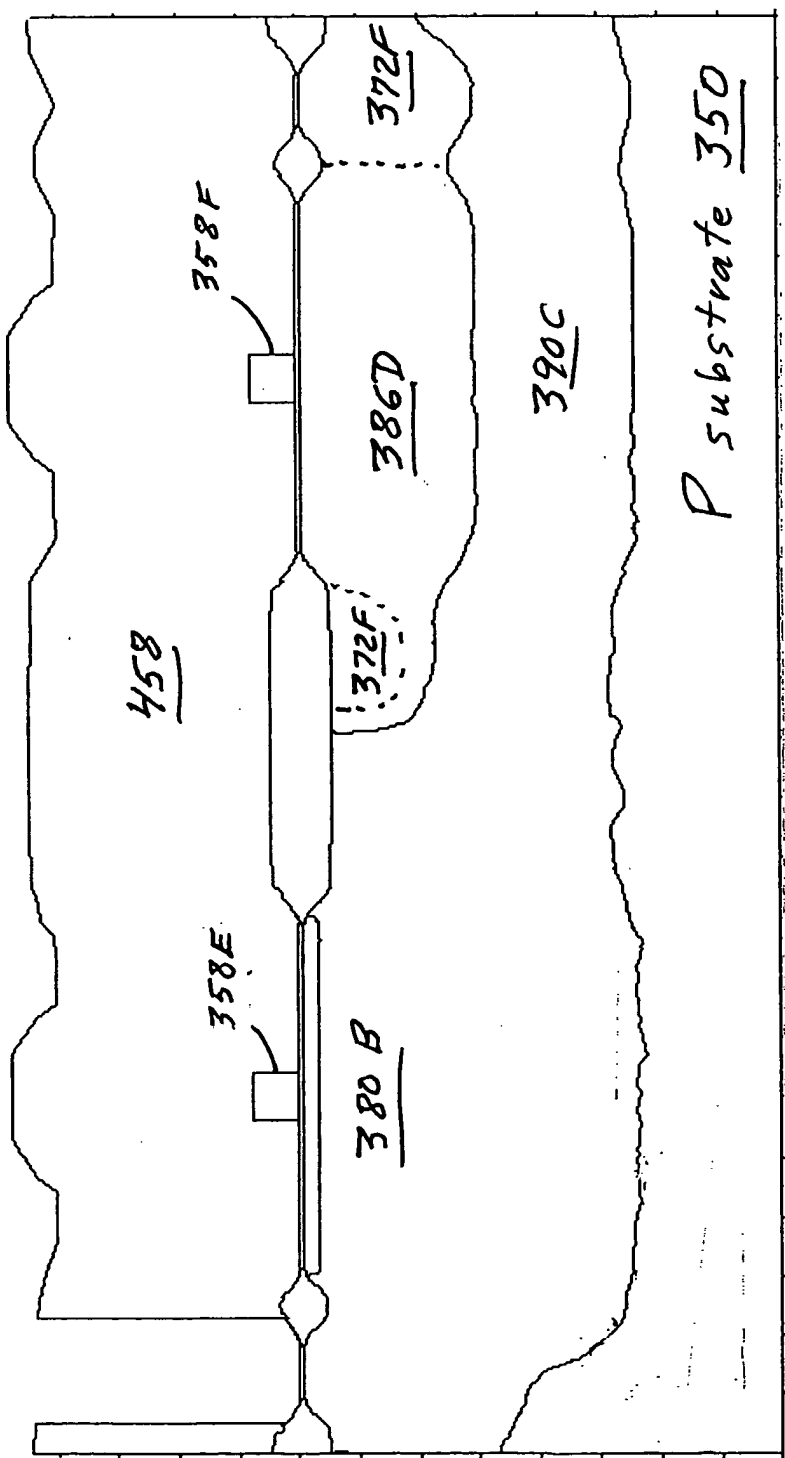


$P_{\text{substrate } 350}$

N-Base Mask and Implant

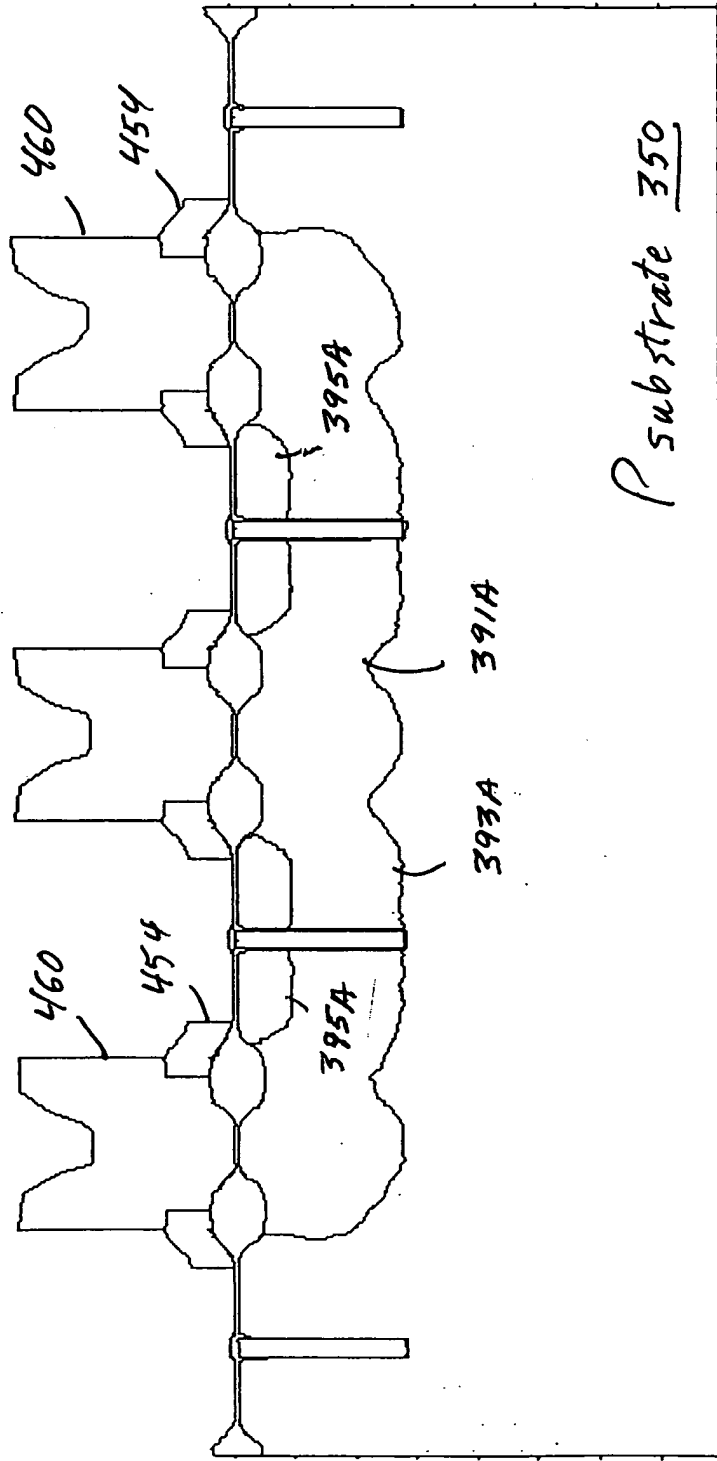
F19. 54D

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



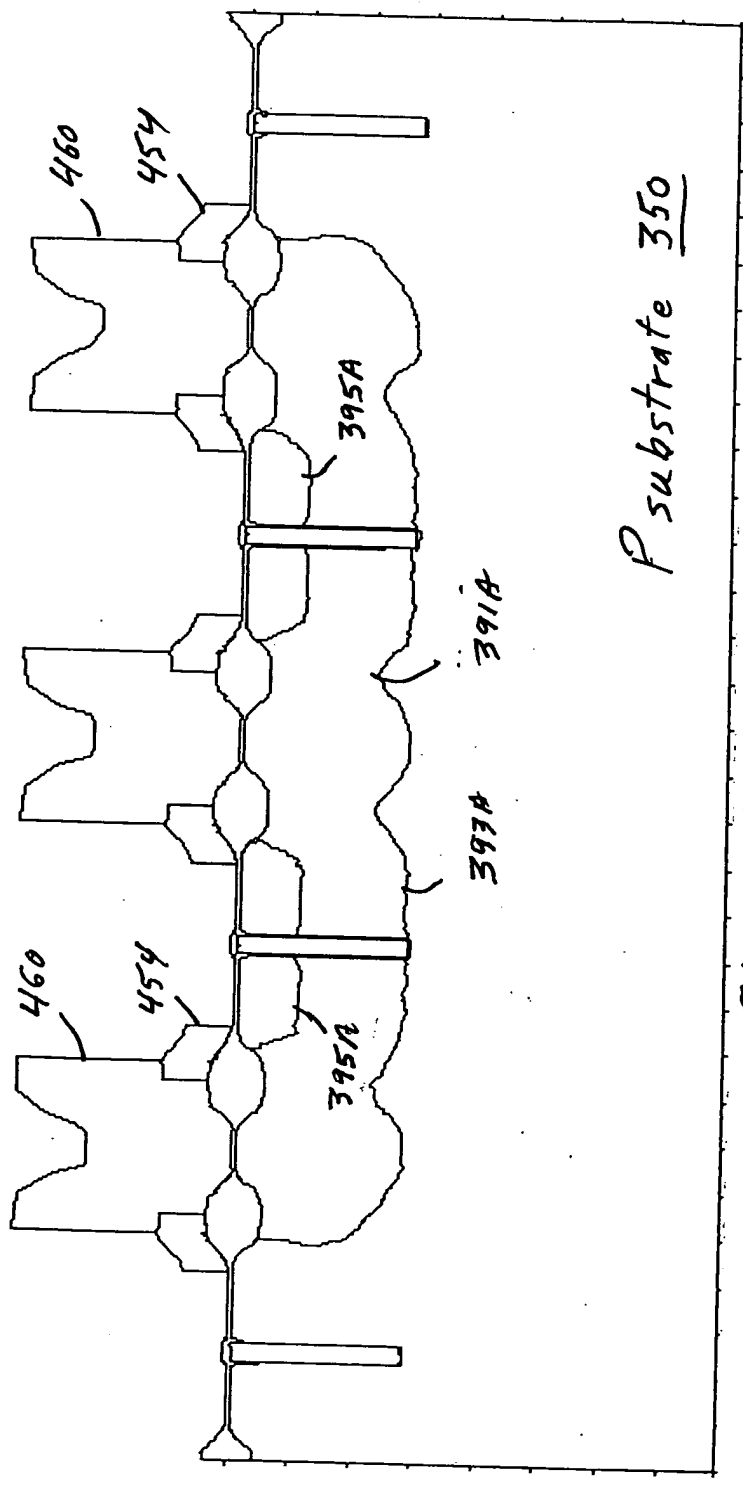
N-Base Mask and Implant
Fig. 54E

30V Lateral Trench DMOS 308



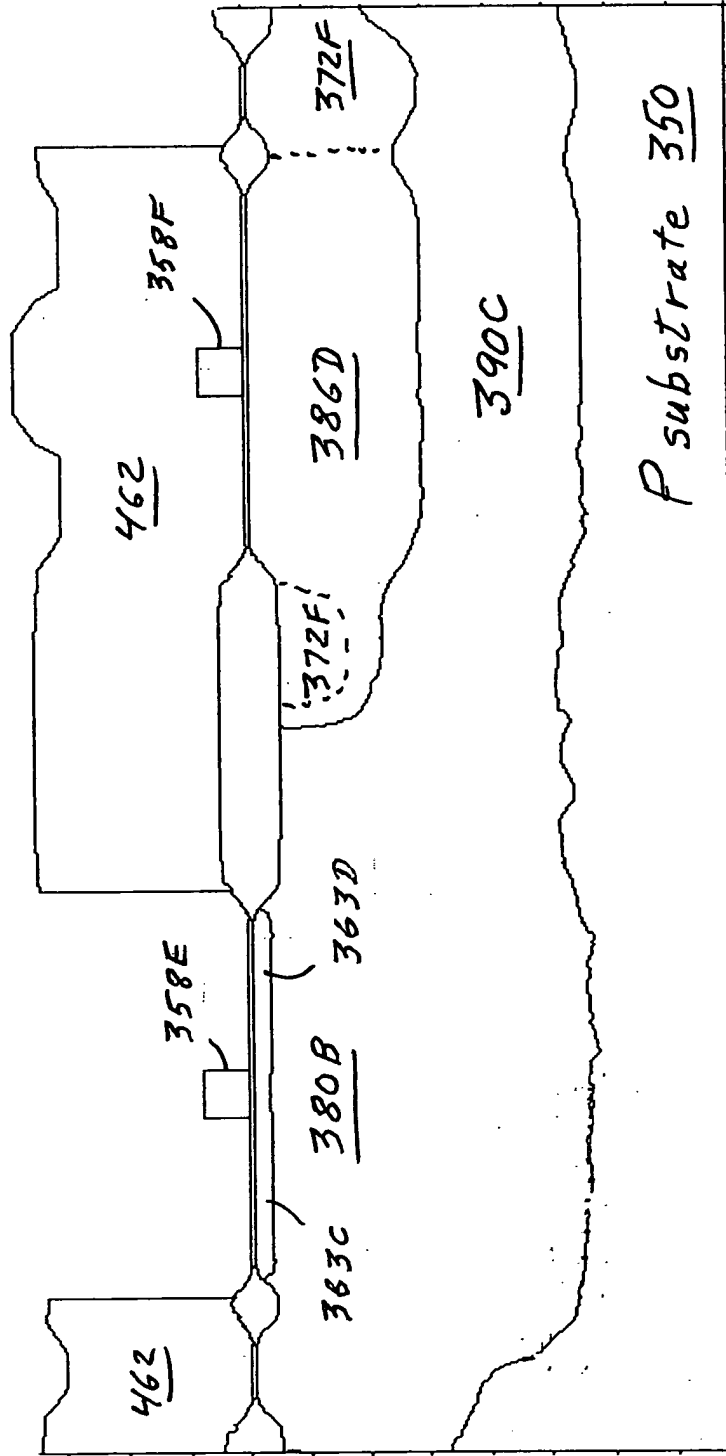
P Body Mask and Implant - First Stage
Fig. 55D

30V Lateral Trench DMOS 308



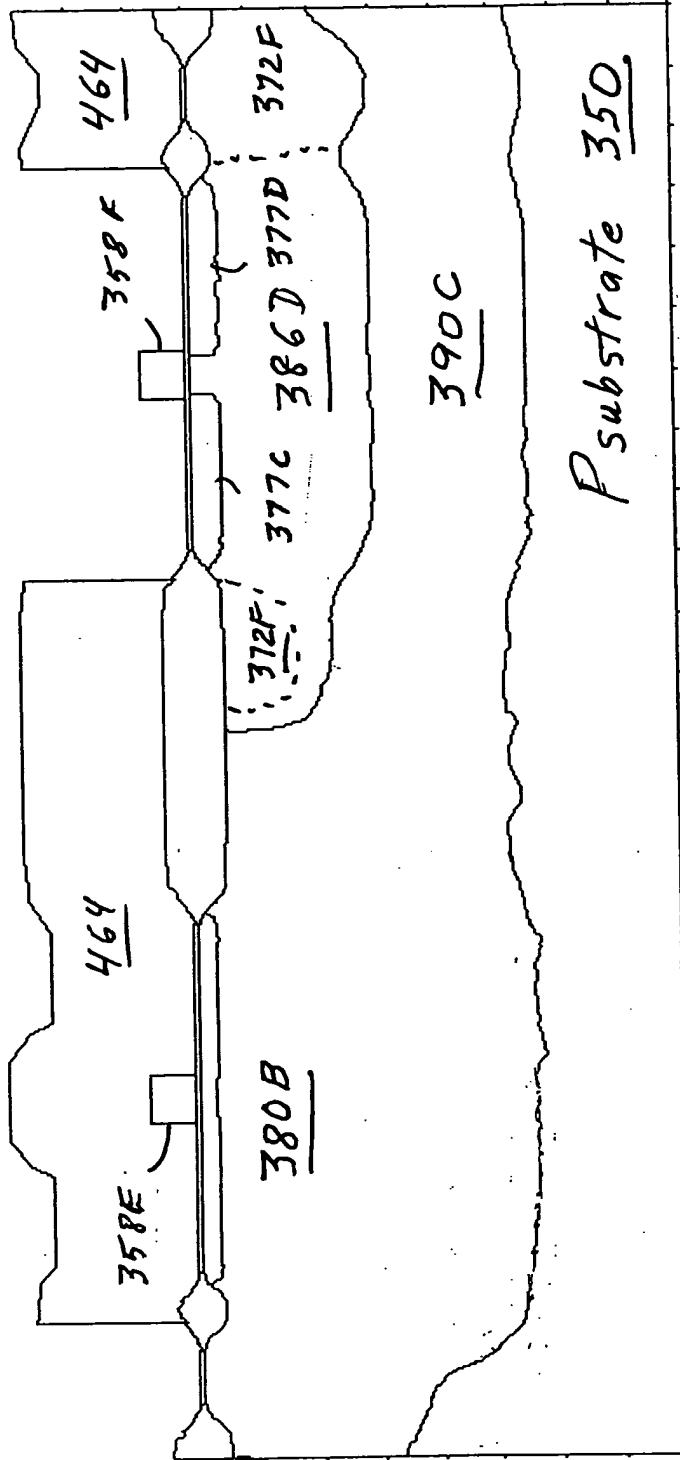
P-body Mask and Implant - Second Stage
Fig. 56D

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



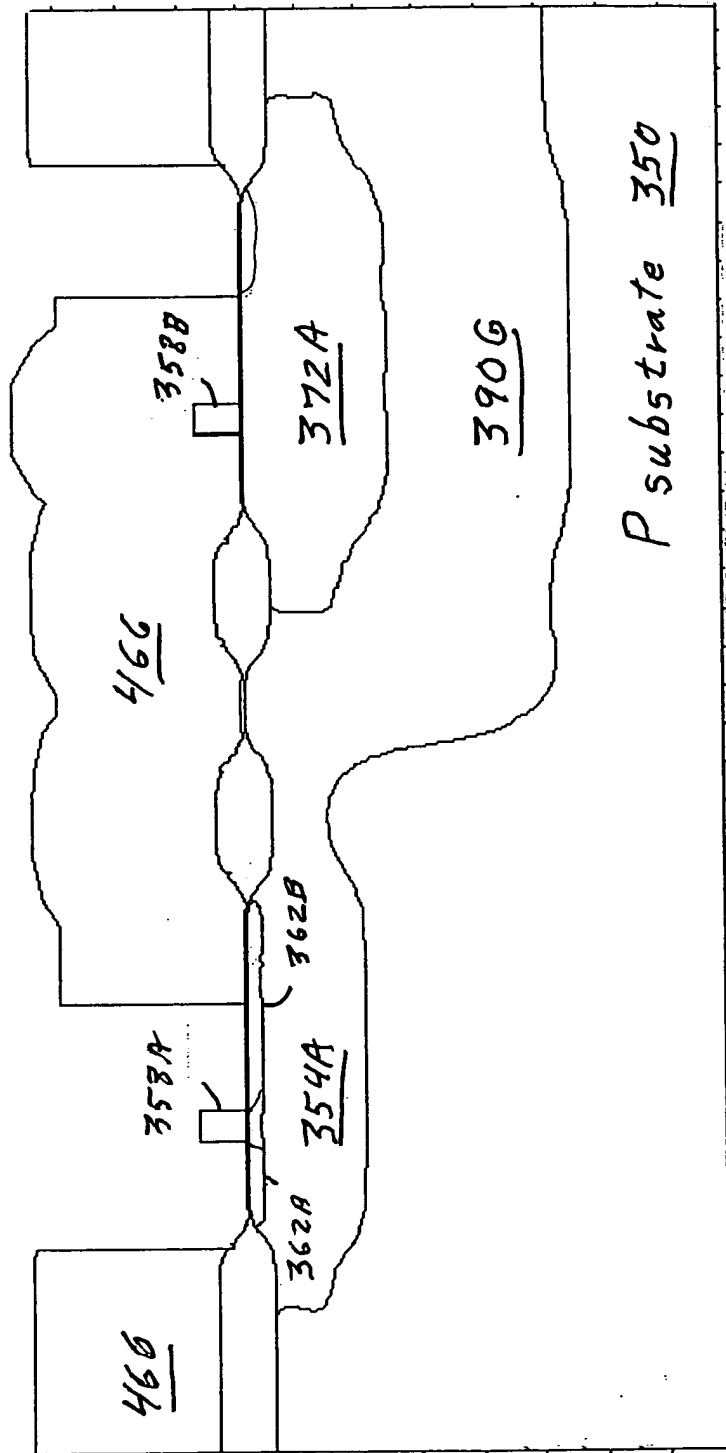
12V PLDD Implant
 Fig. 57E

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



12V N-LDD Implant
Fig. 58E

5V PMOS 301 5V NMOS 302

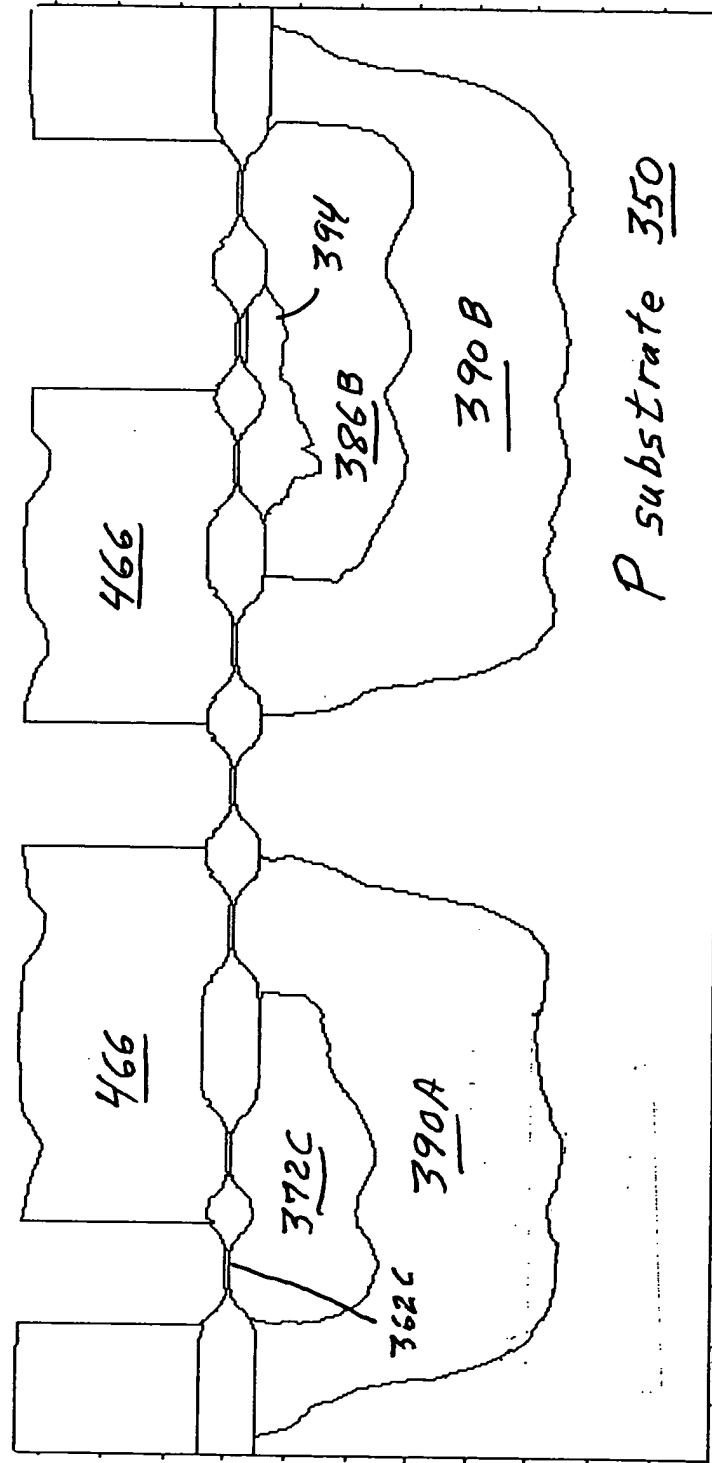


5V PLDD Implant
Fig. 59A

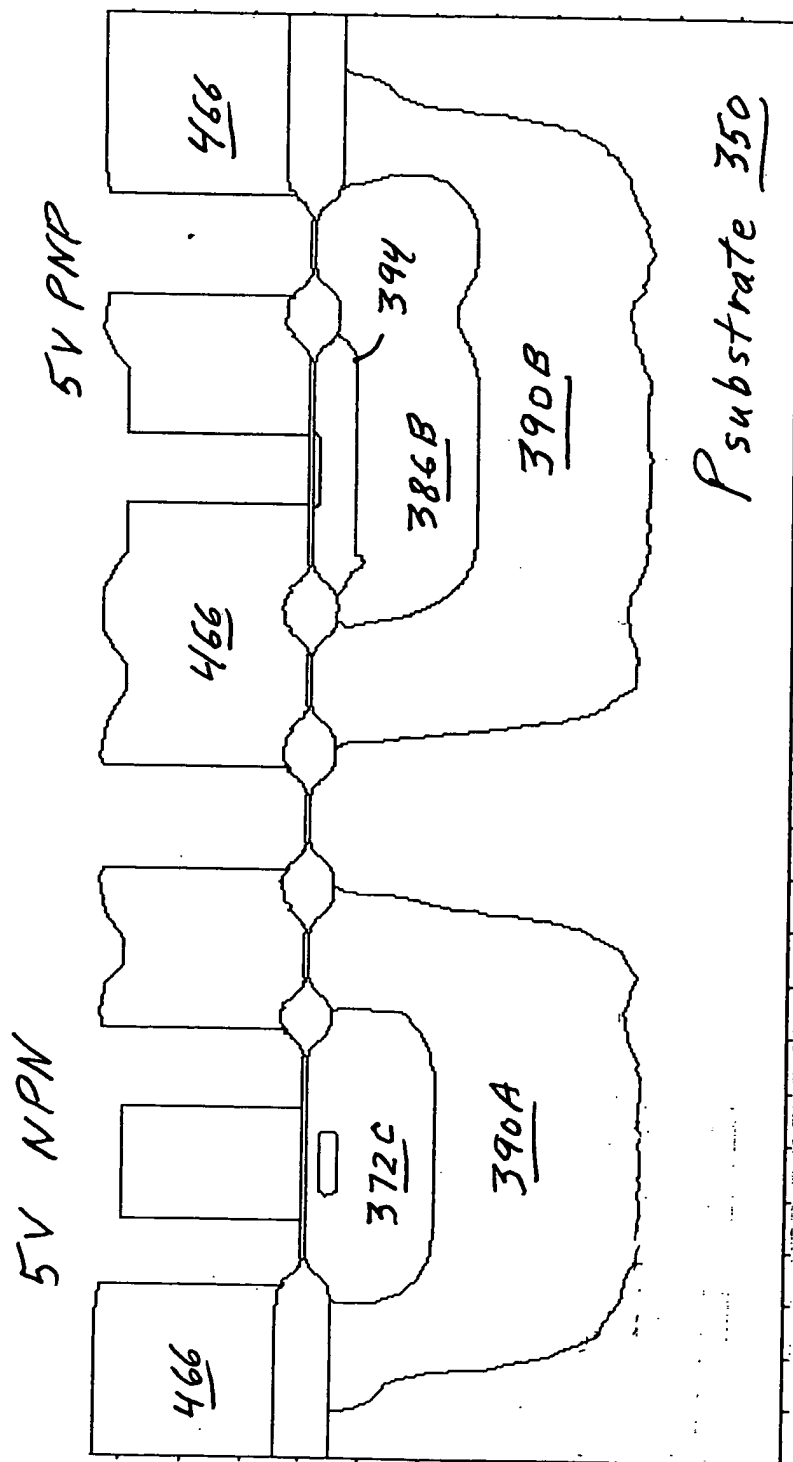
High F_T Layout

5V NPN 305

5V PNP 306

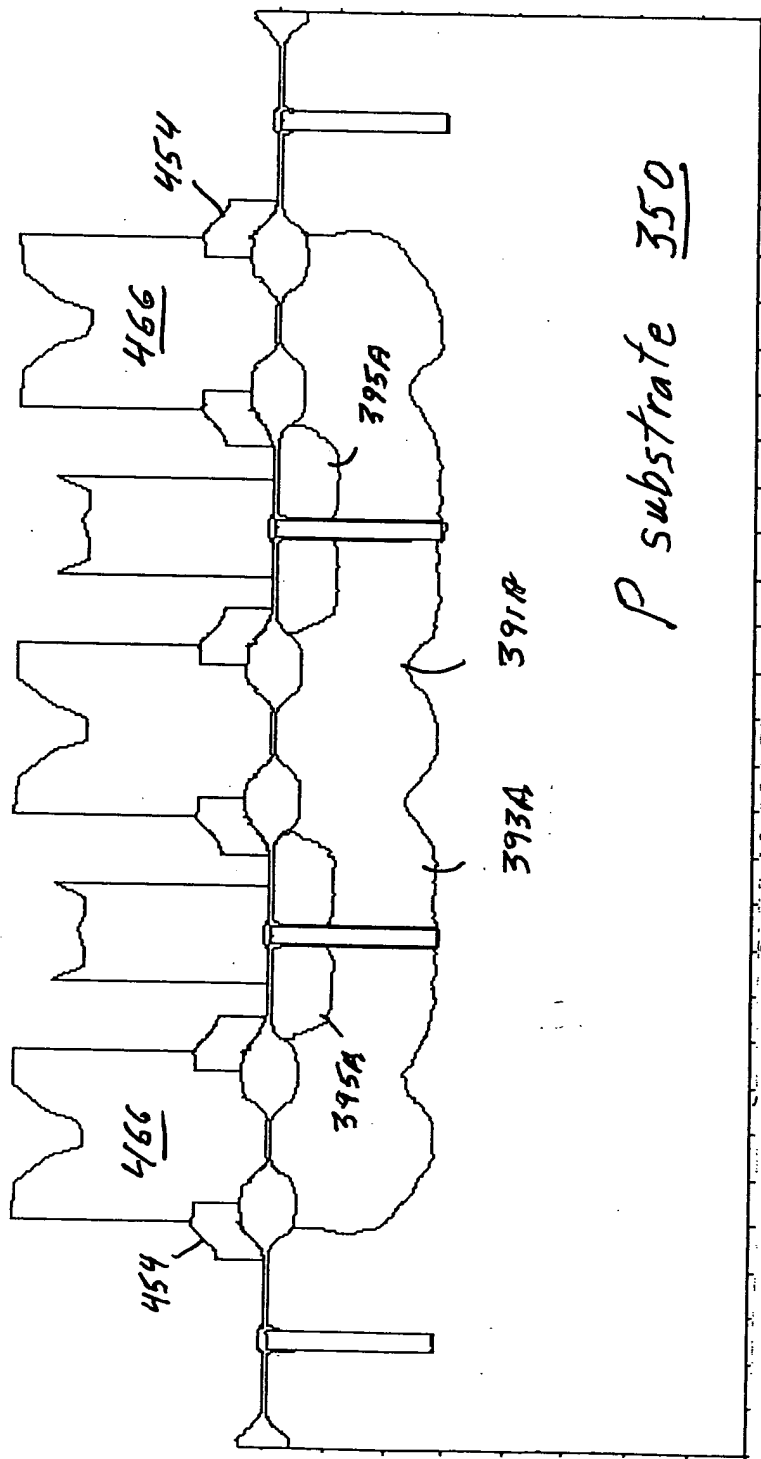
5V P-LDD Implant
Fig. 59B

Conventional Layout



5V P-LDD Implant
Fig. 59C

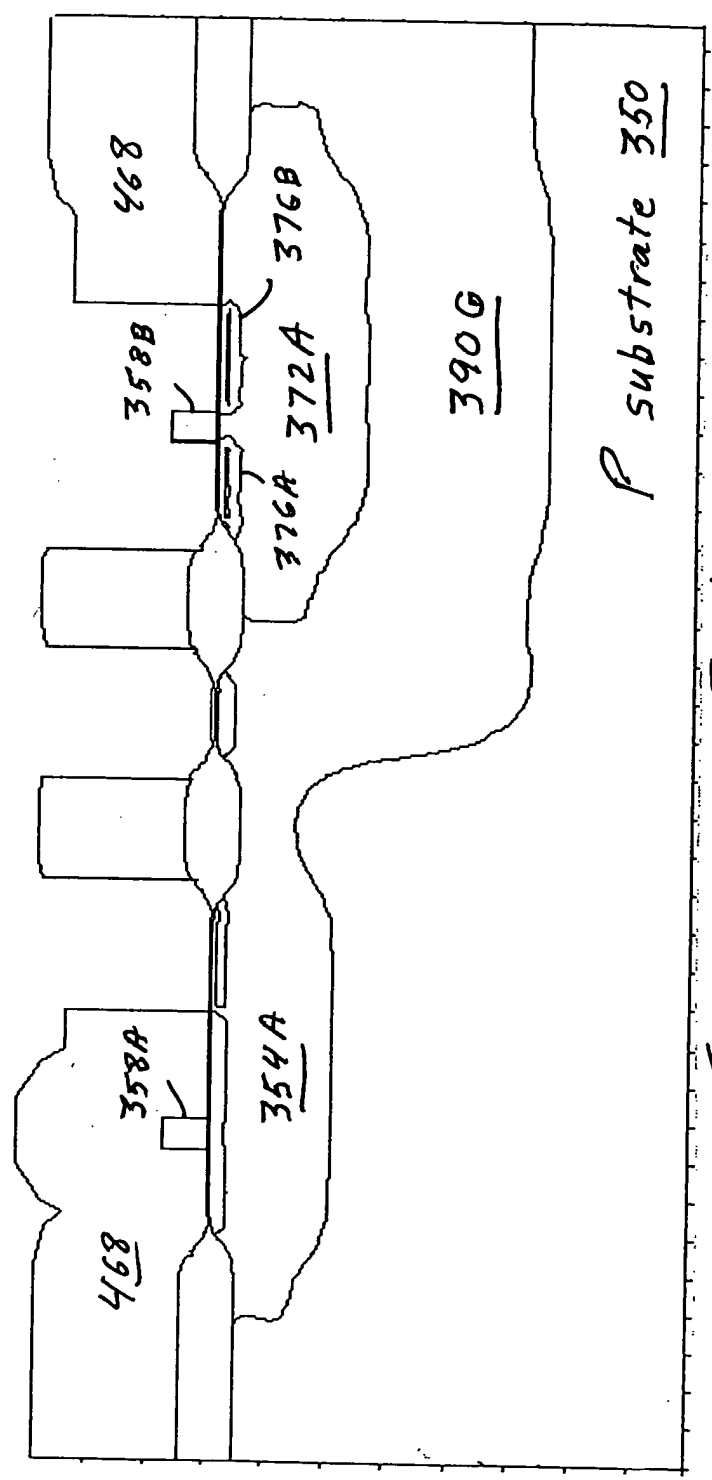
30V Lateral Trench DMOS 308



P substrate 350

5V P-LDD Implant
Fig. 59D

5V PMOS 301 5V NMOS 302



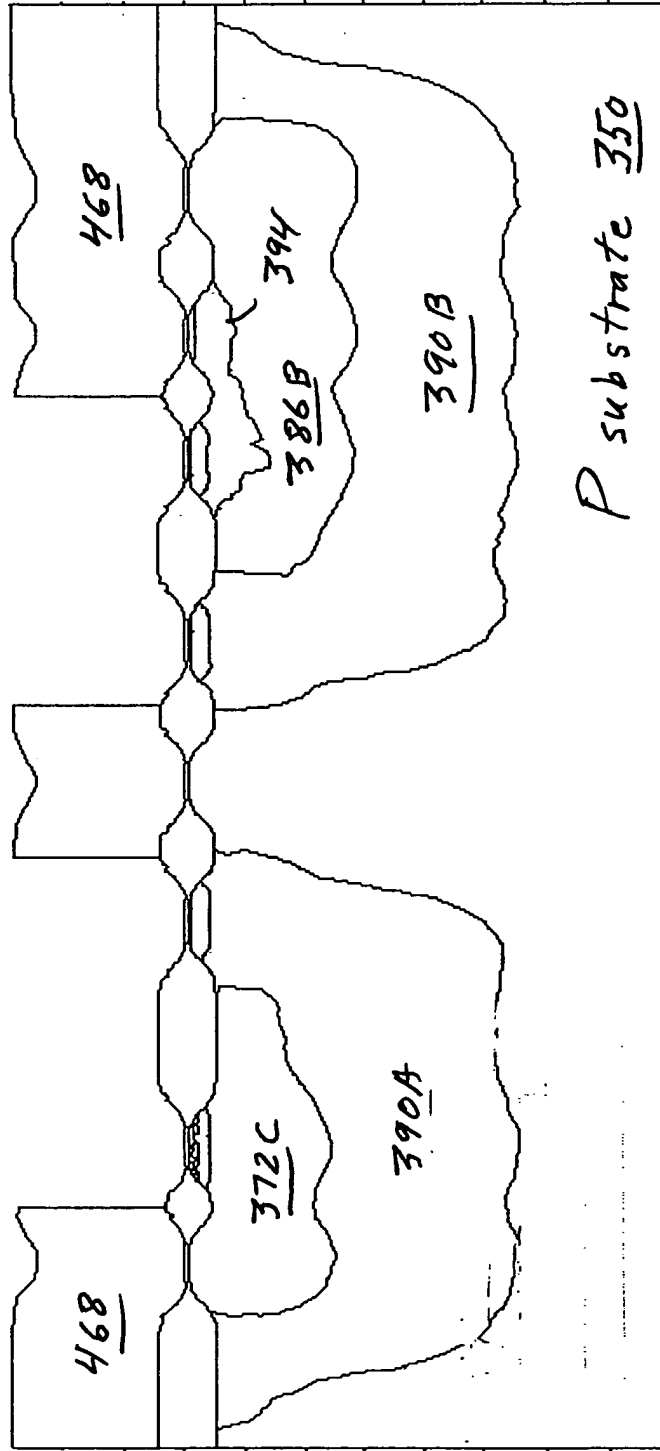
5V N-LDD Implant
Fig. 60A

179/219

High F_T Layout

5V NPN 305

5V PNP 306

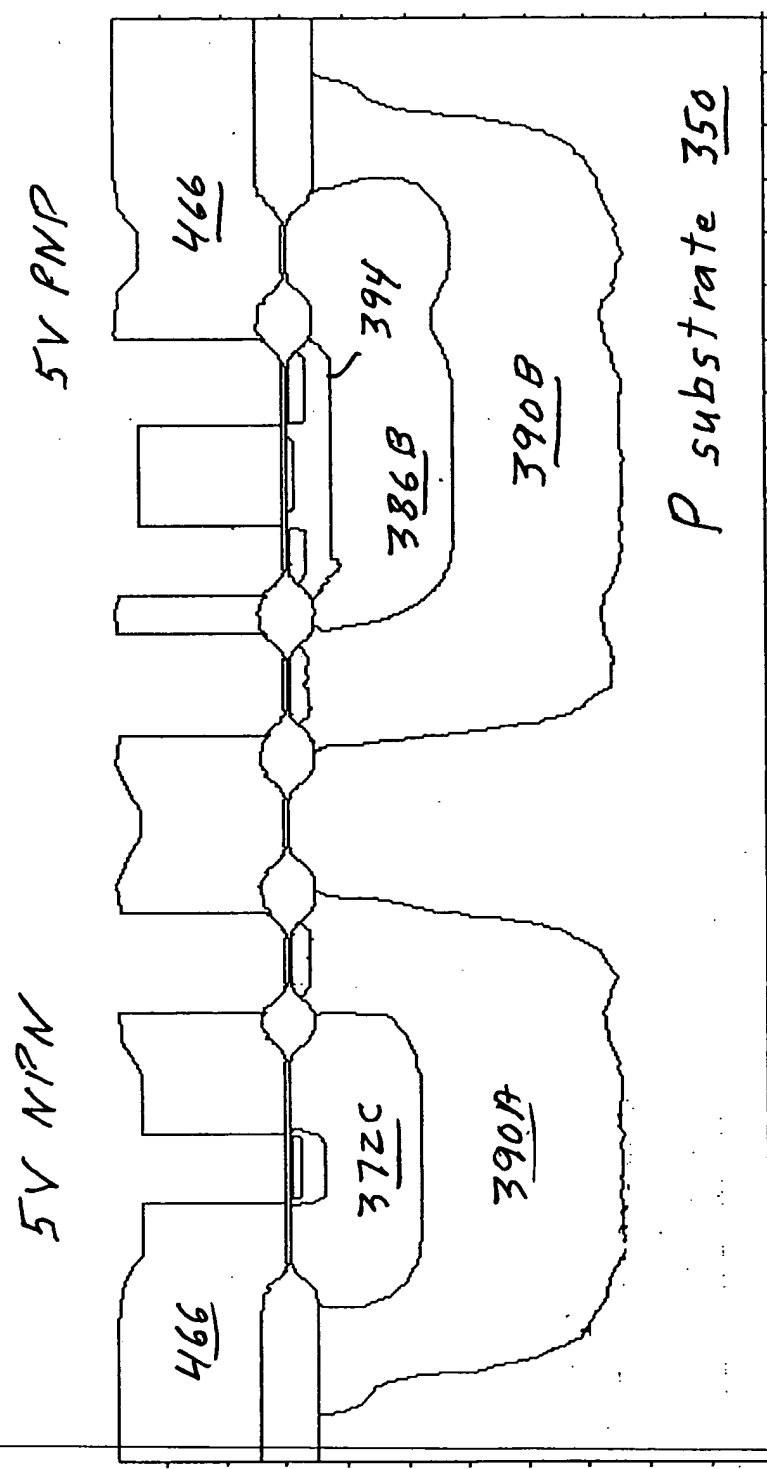


P substrate 350

5V N-LDD Implant

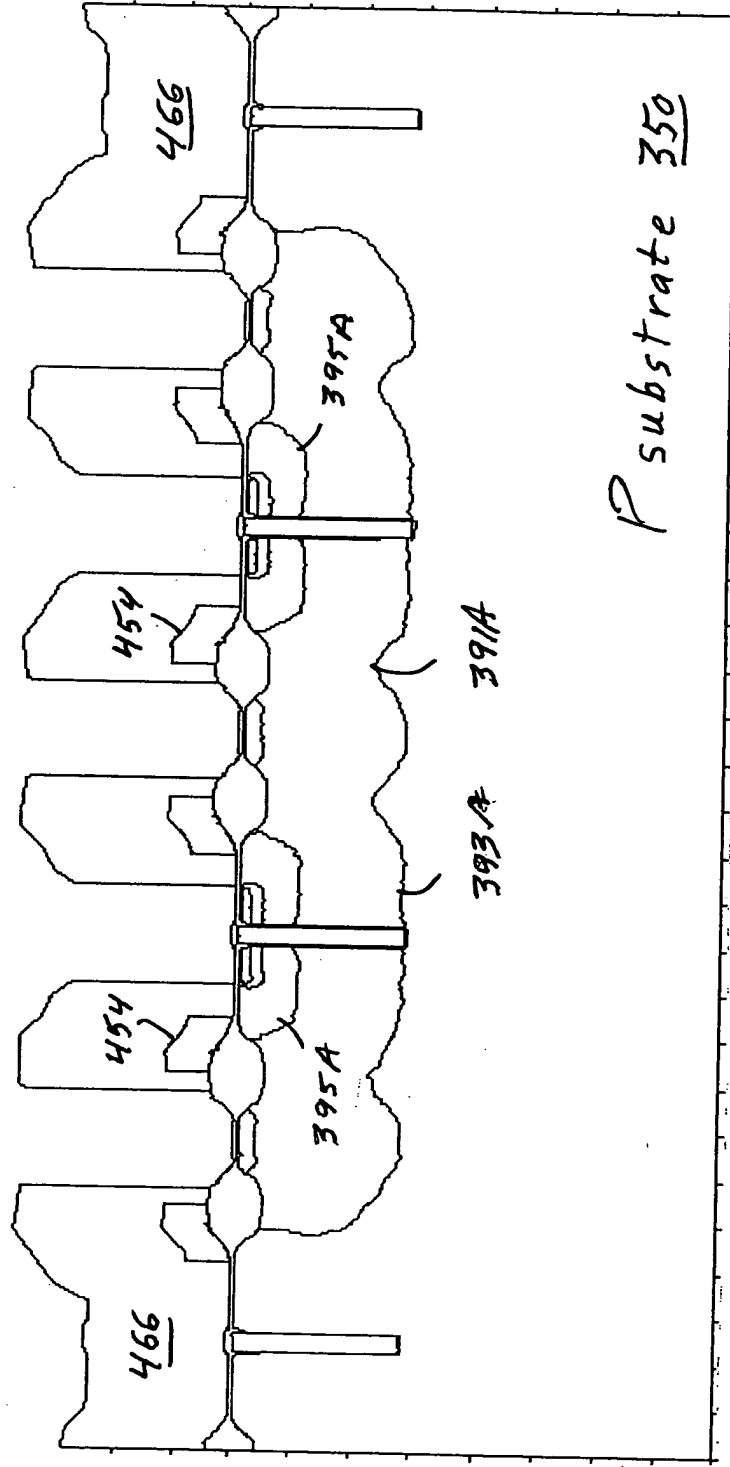
Fig 60B

Conventional Layout



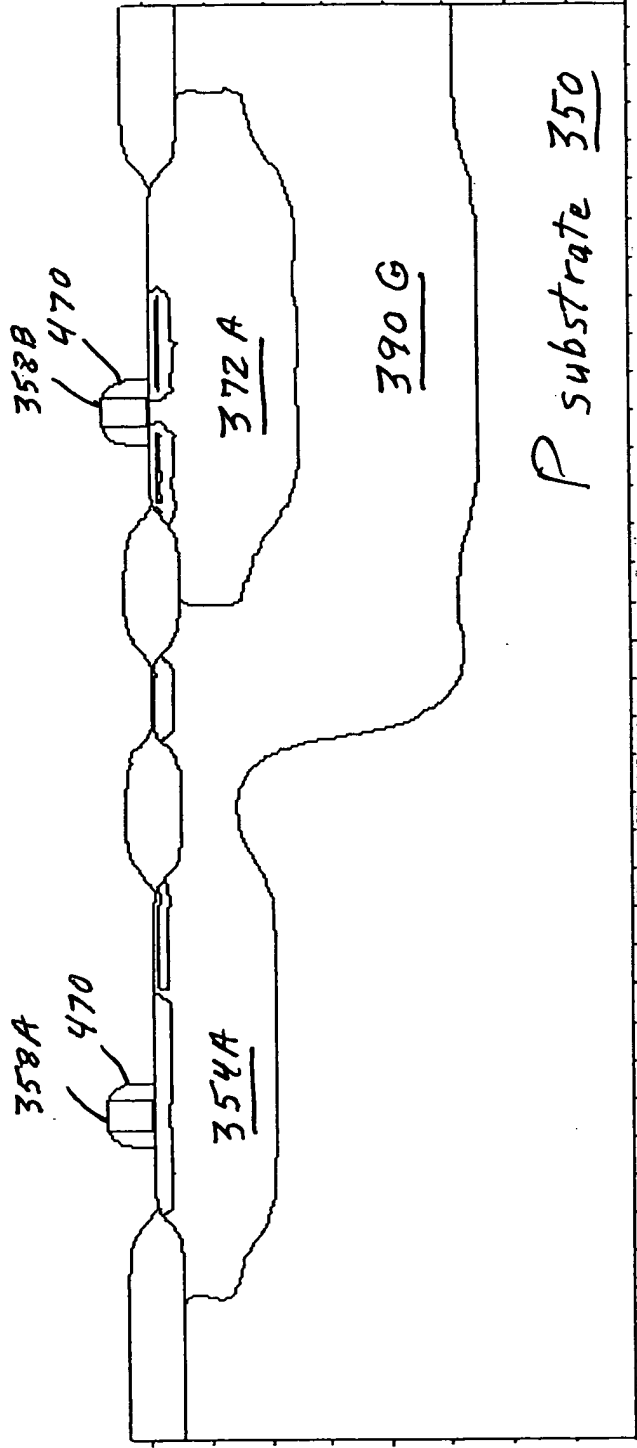
5V N-LDD Implant
Fig. 60C

30V Lateral Trench DMOS 308



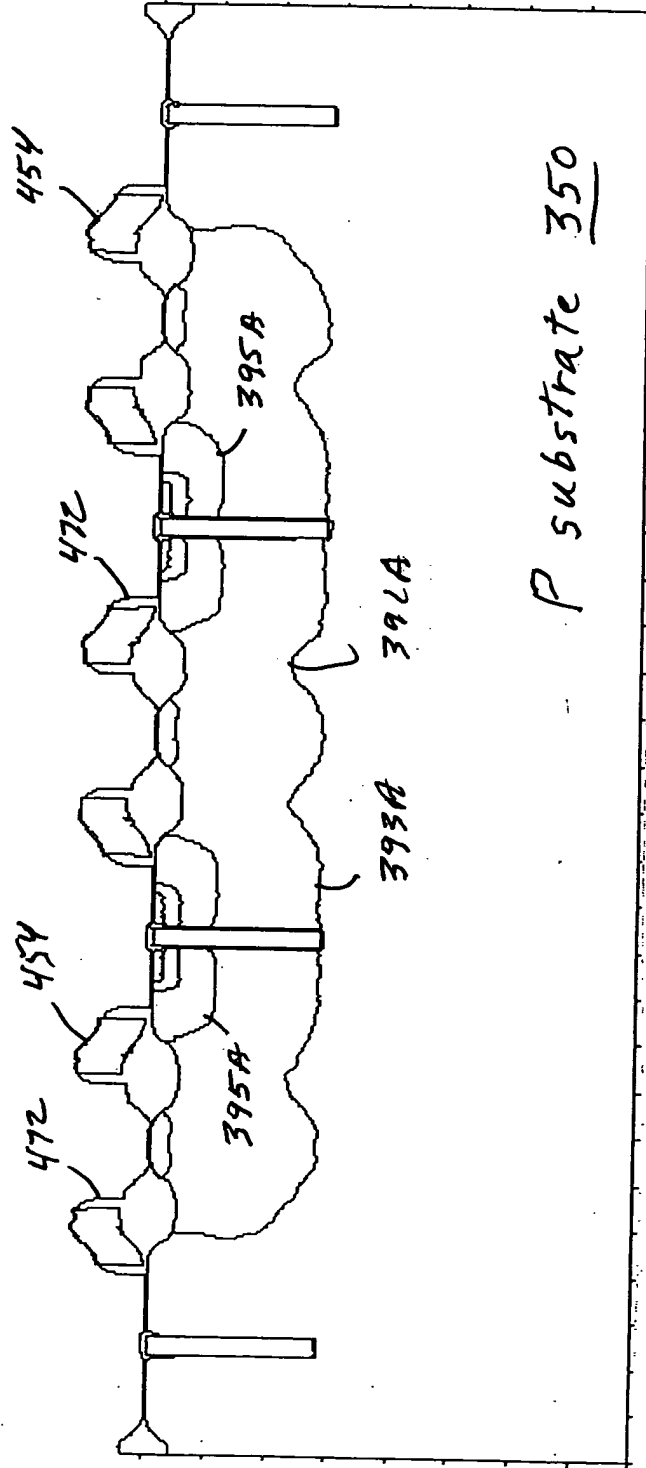
5V N-LDD Implant
Fig. 60D

5V PMOS 301 5V NMOS 302



Sidewall Spacers
Fig. 61A

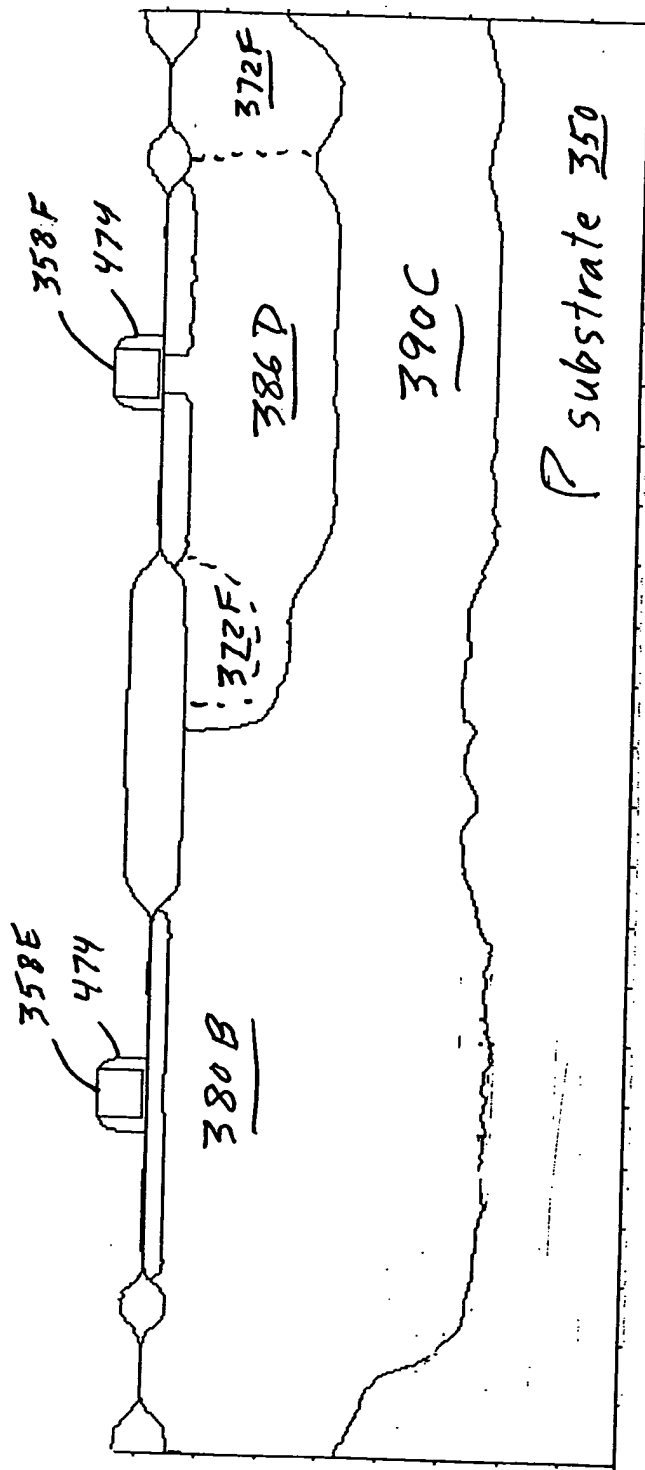
30V Lateral Trench DMOS 308



Side wall Spacers

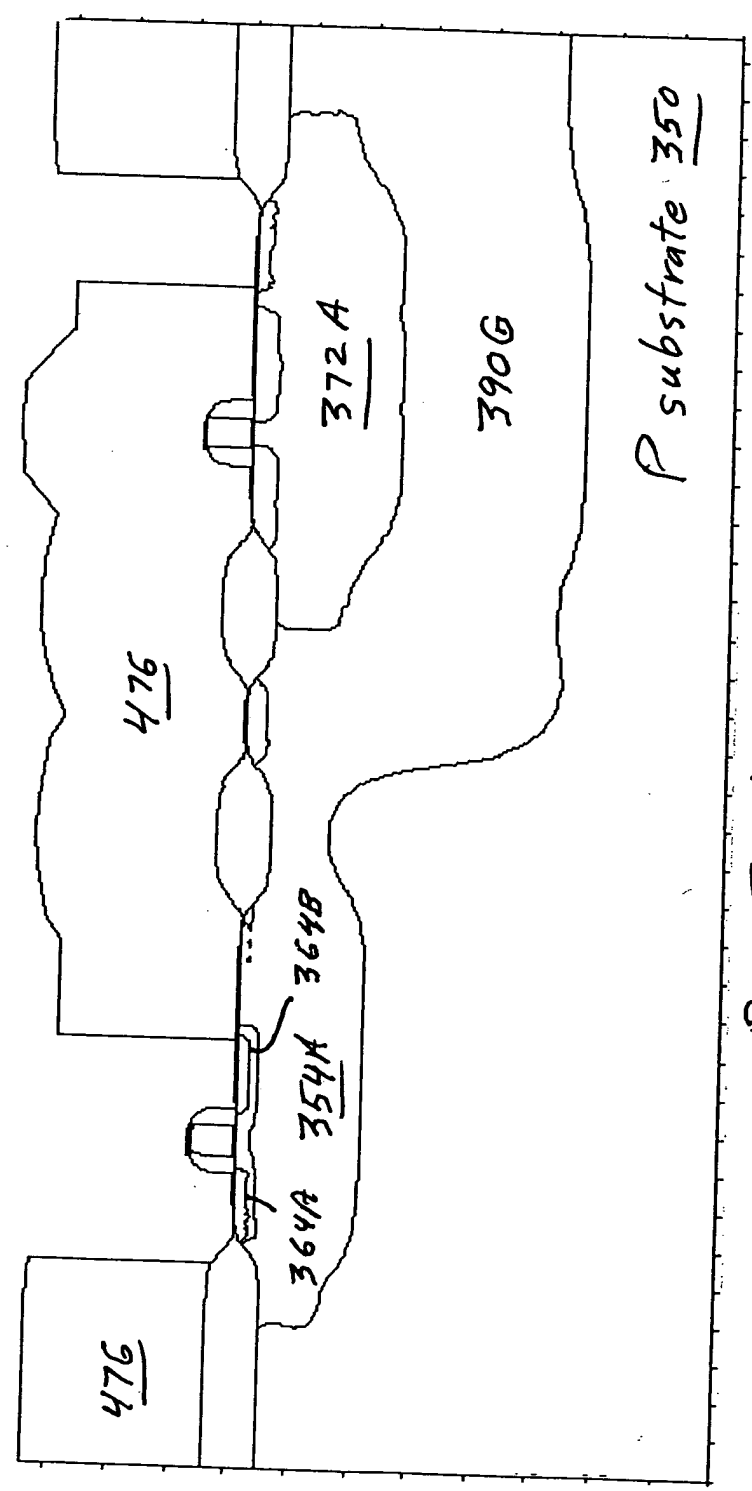
Fig. 61D

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



Sidewall Spacers
 Fig. 61E

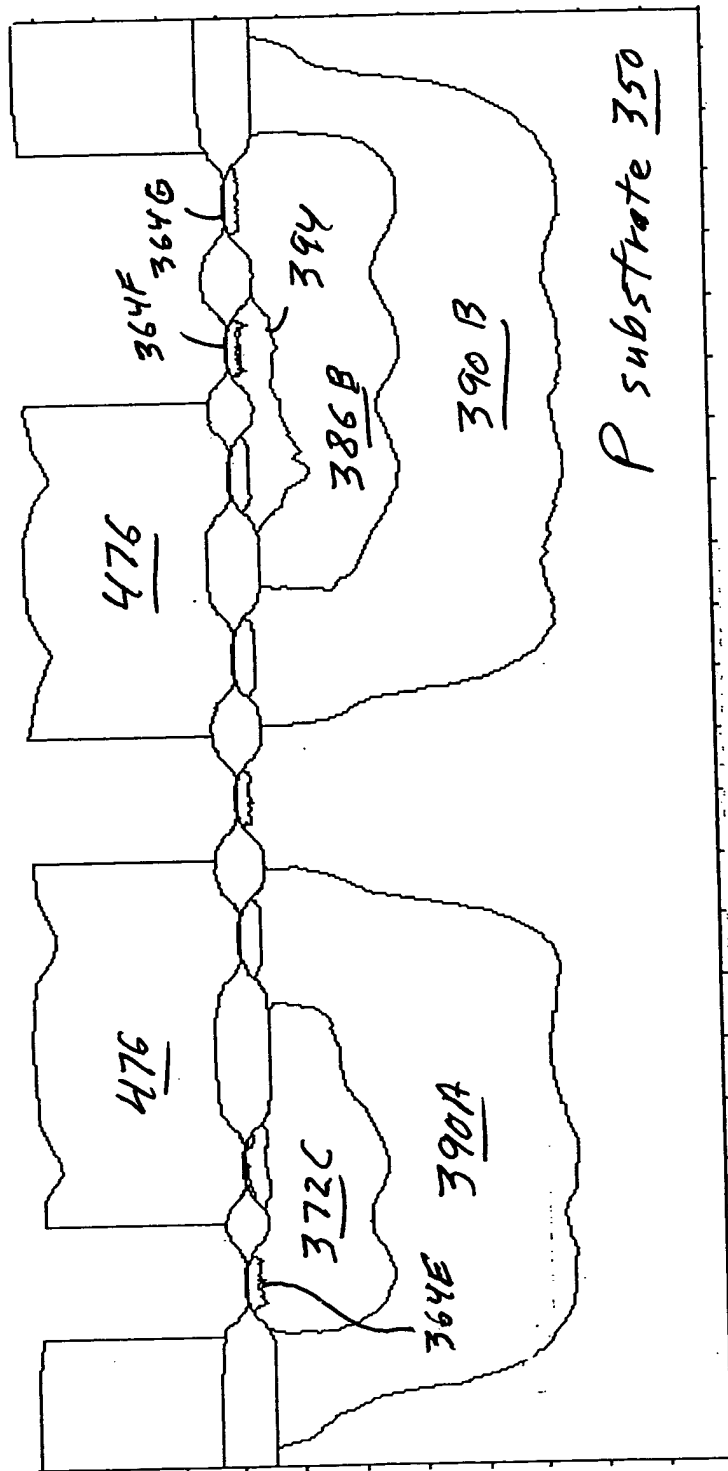
5V PMOS 301 5V NMOS 302



Pt Implant
Fig. 62A

High F_T Layout

5V NPN 305 5V PNP 306

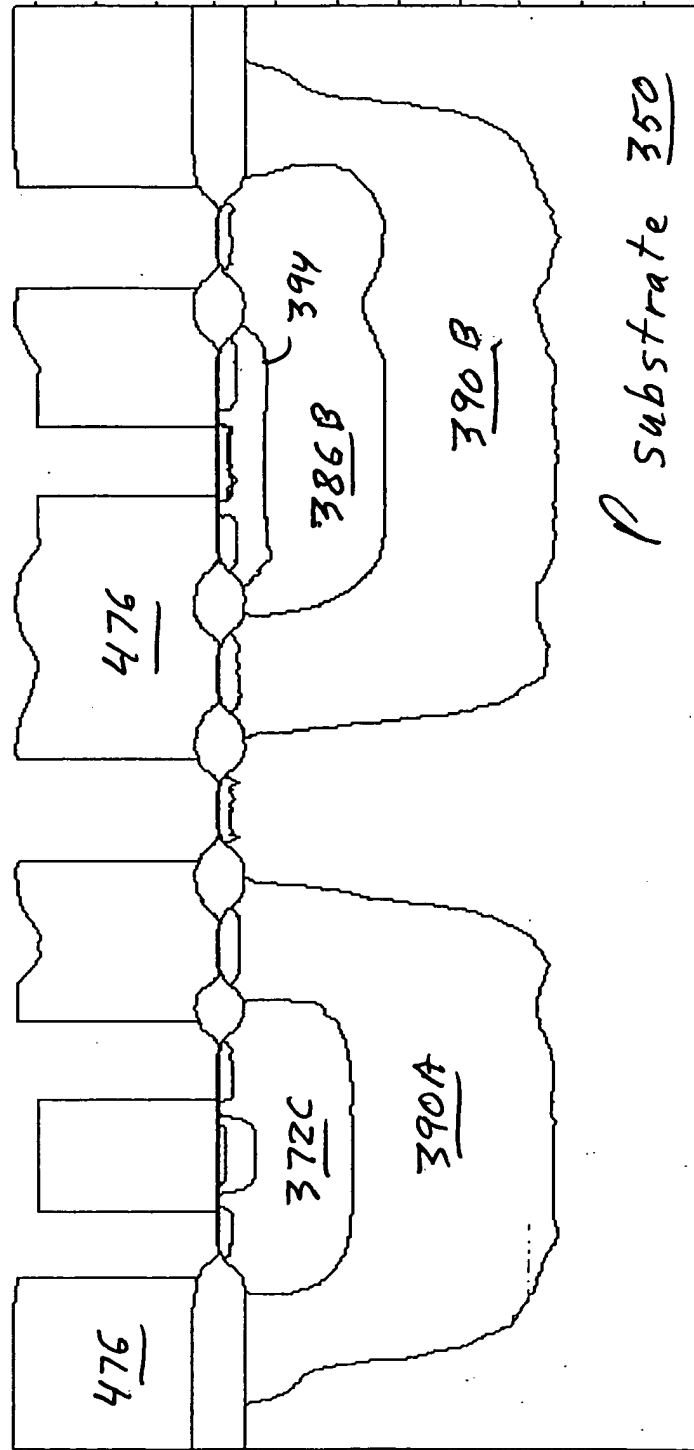


P+ Implant
Fig. 62B

Conventional Layout

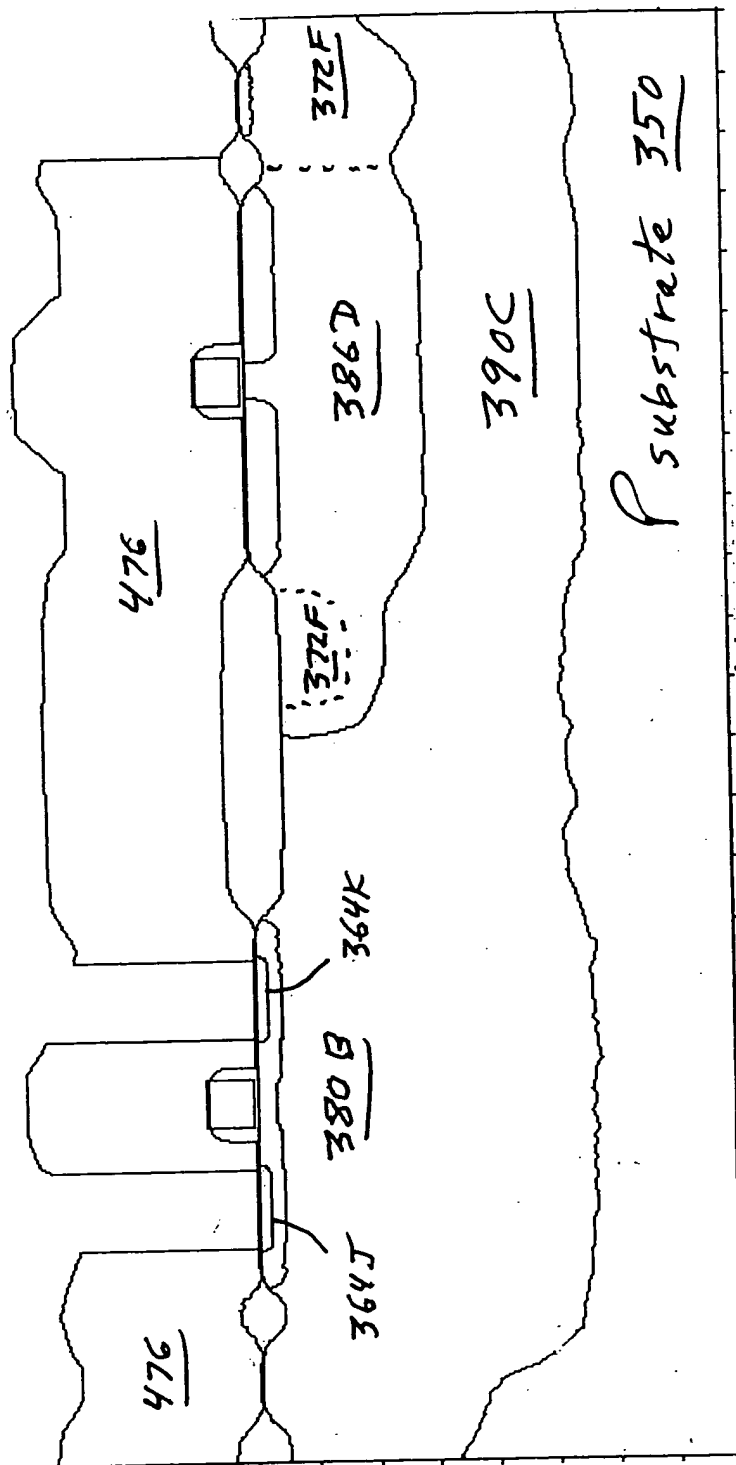
5V NPN

5 PNP



Pt Implant
Fig. 62C

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310

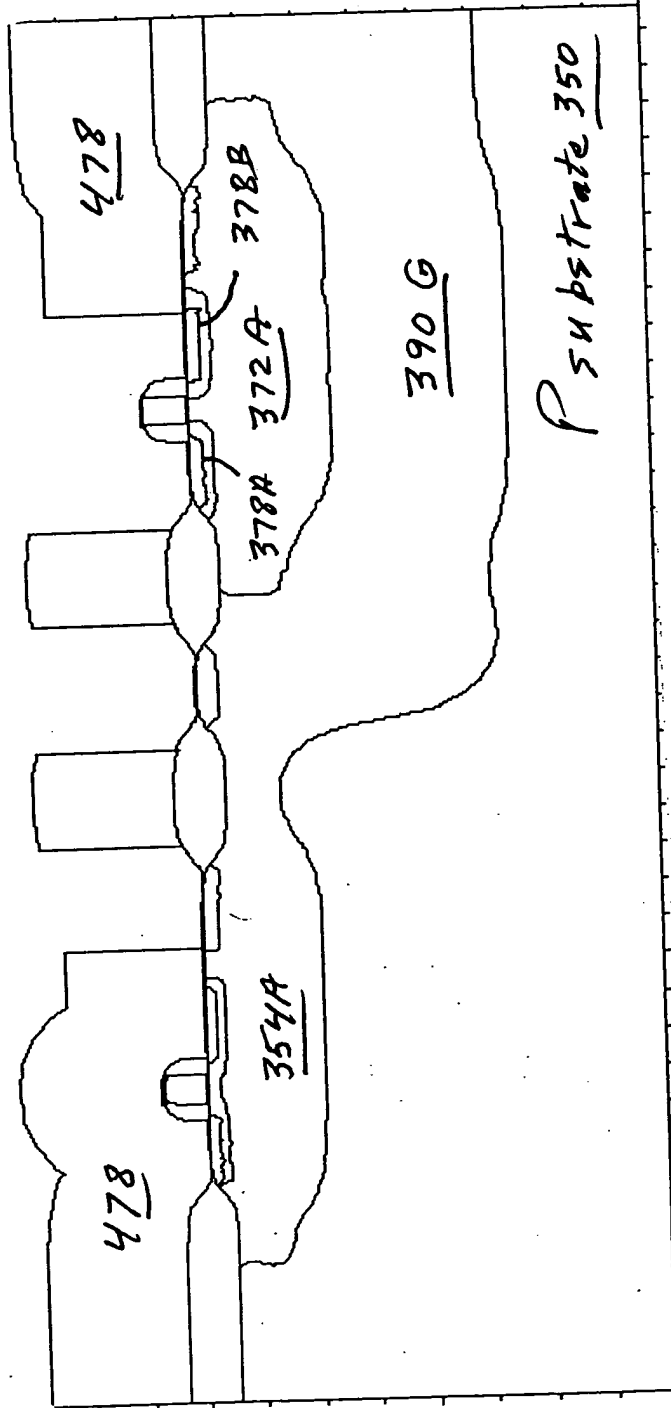


Pt Implant
Fig 62E

190/219

5V NMOS 302

5V PMOS 301

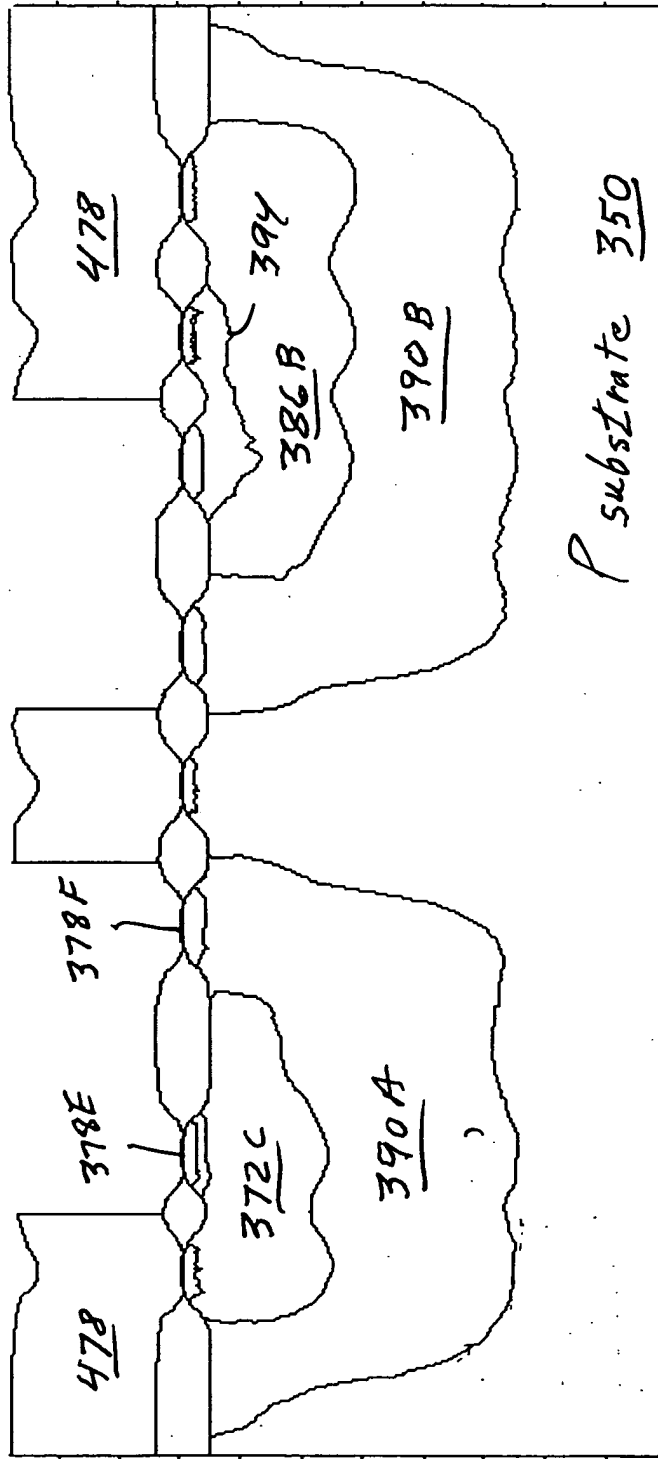


N+ Implant
Fig. 63A

High F_T Layout

5V NPN 305

5V PNP 306



P substrate 350

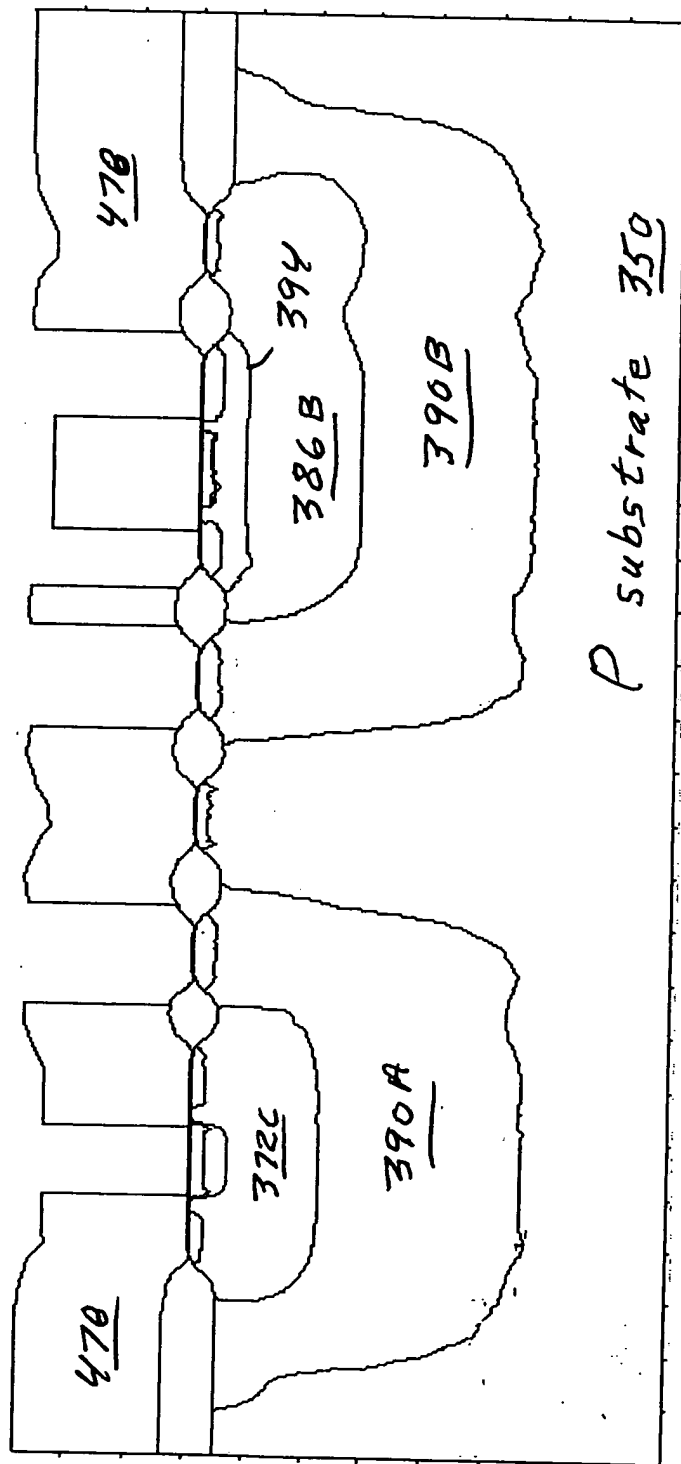
N+ Implant

Fig. 63B

Conventional Layout

5V NPN

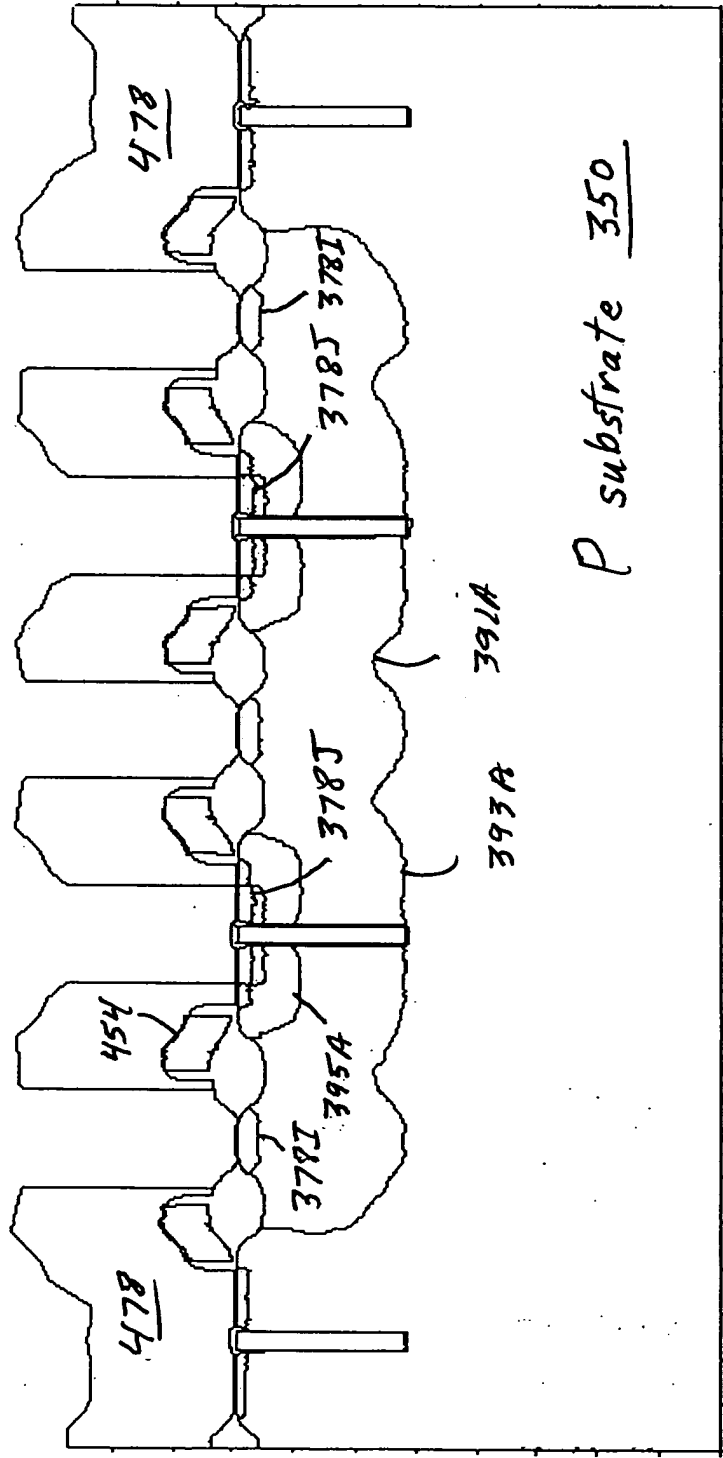
5V PNP



Nt Implant

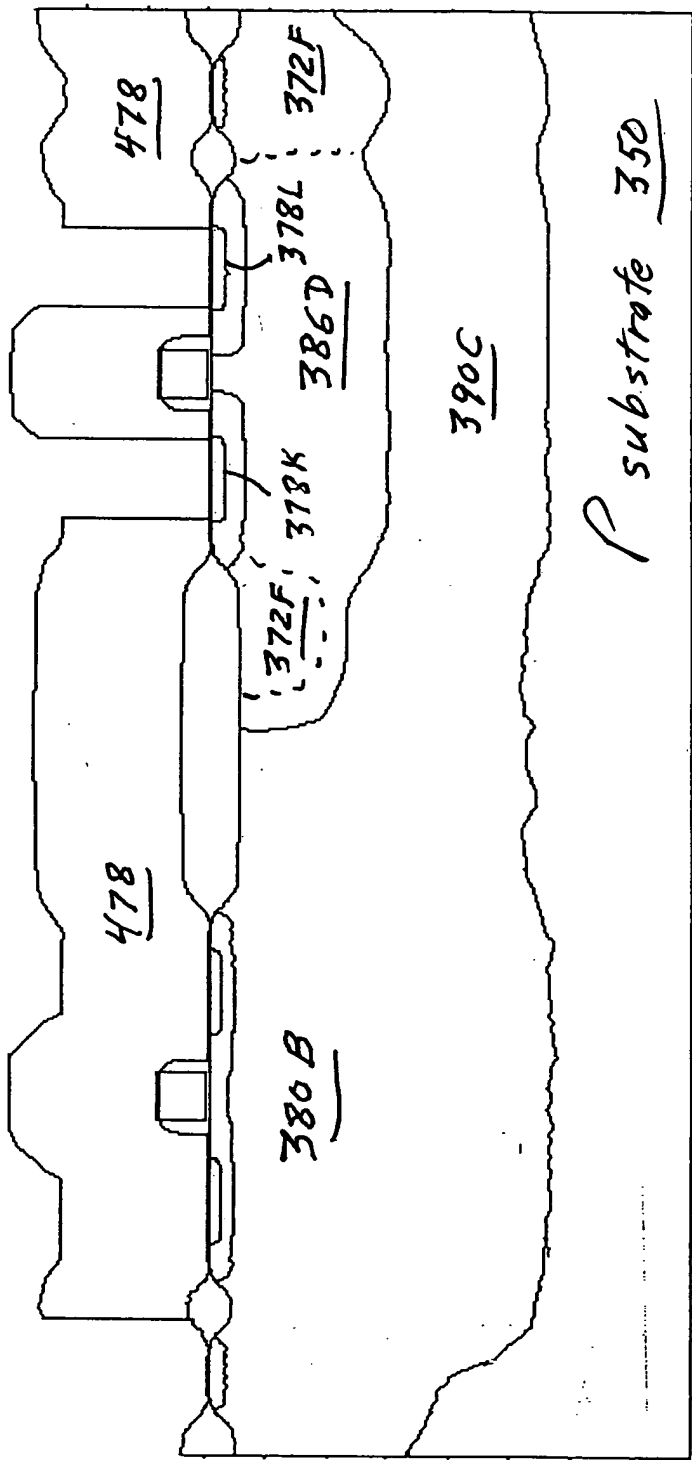
Fig. 63C

30V Lateral Trench DMOS 308

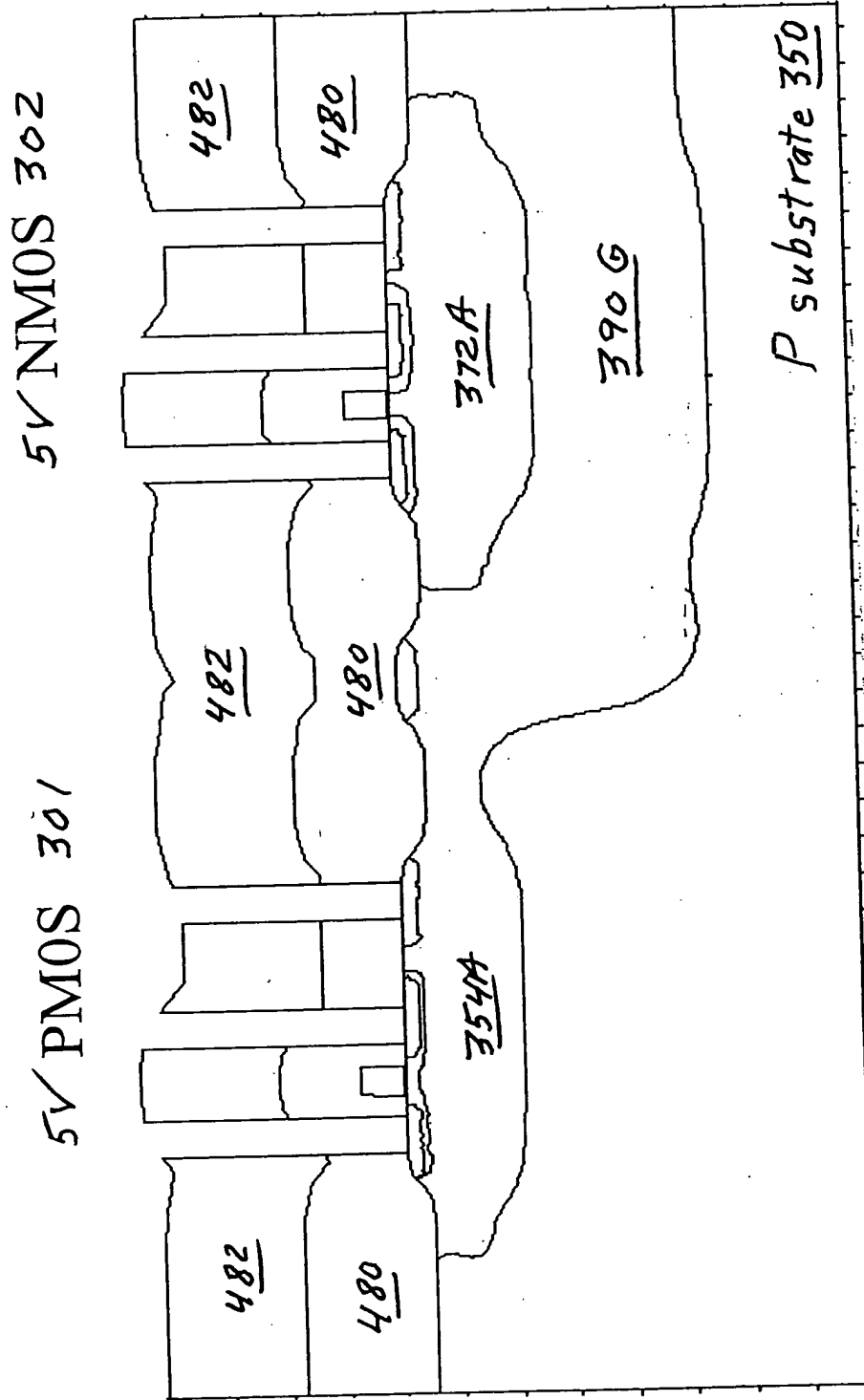


N+ Implant
Fig 63D

Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



N+ Implant
Fig 63E



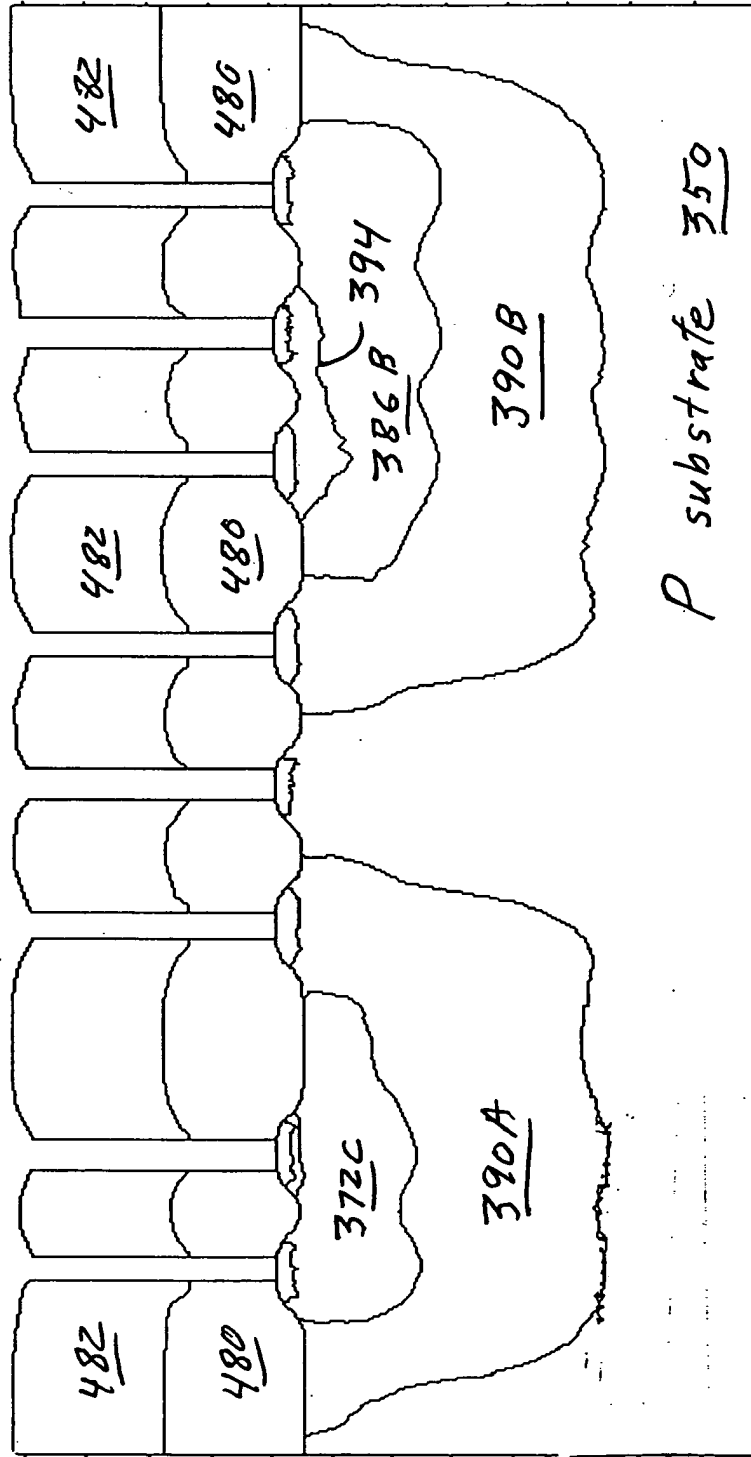
Interlayer Dielectric Deposition and Etch
Fig. 64A

196/219

High F_T Layout

5V NPN 305

5V NPN 306



Interlayer Dielectric Deposition and Etch

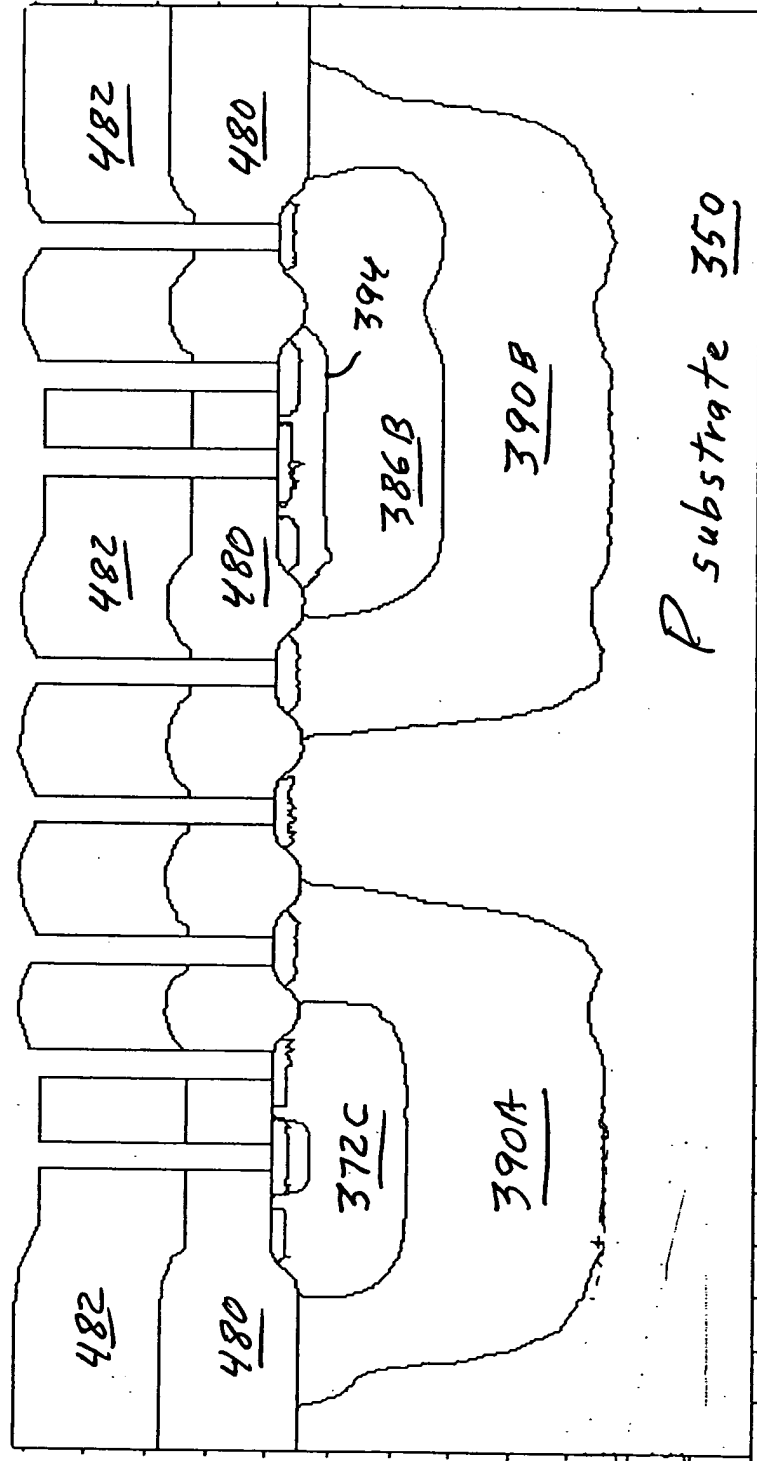
Fig. 64B

197/219

Conventional Layout

5V NPN

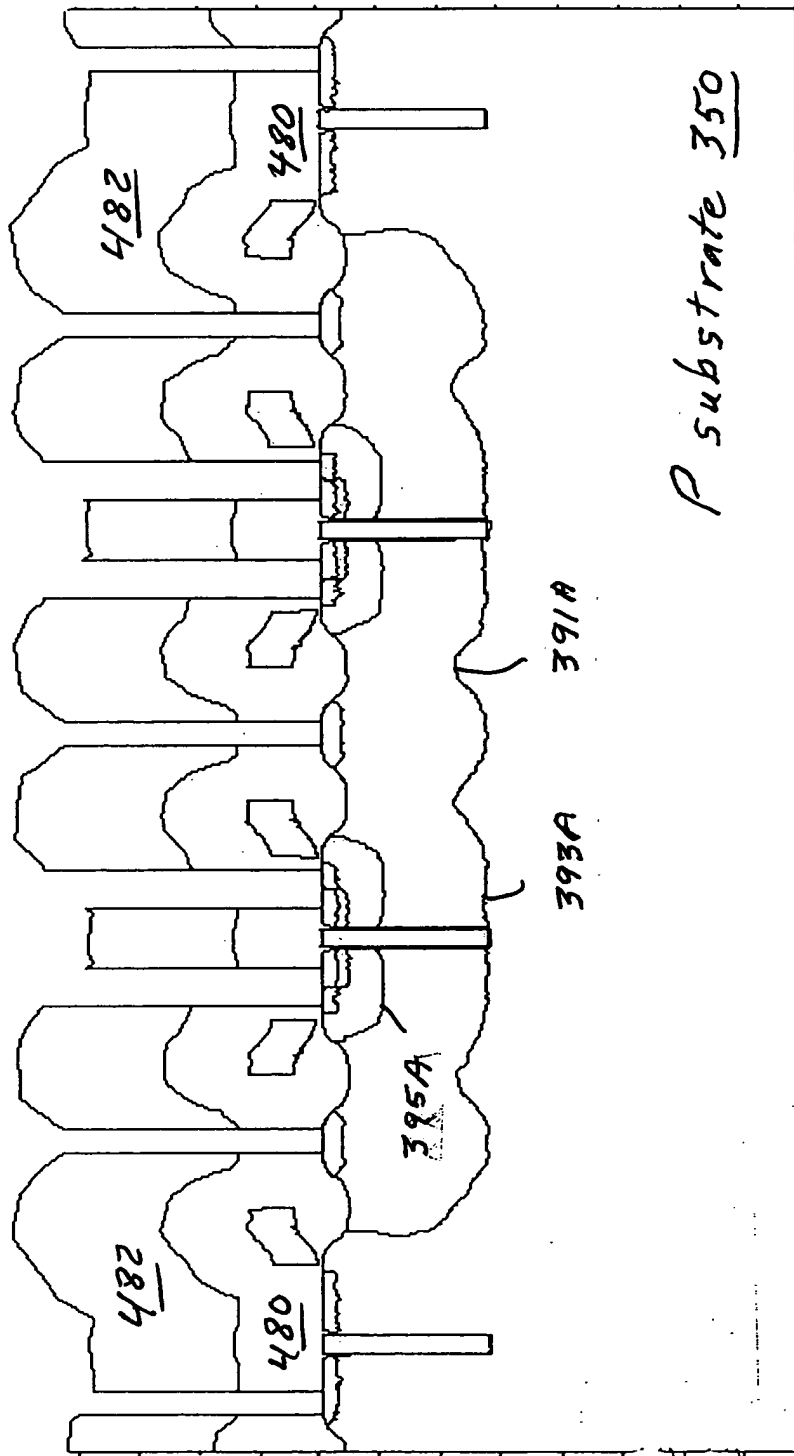
5V PNP



P substrate 350

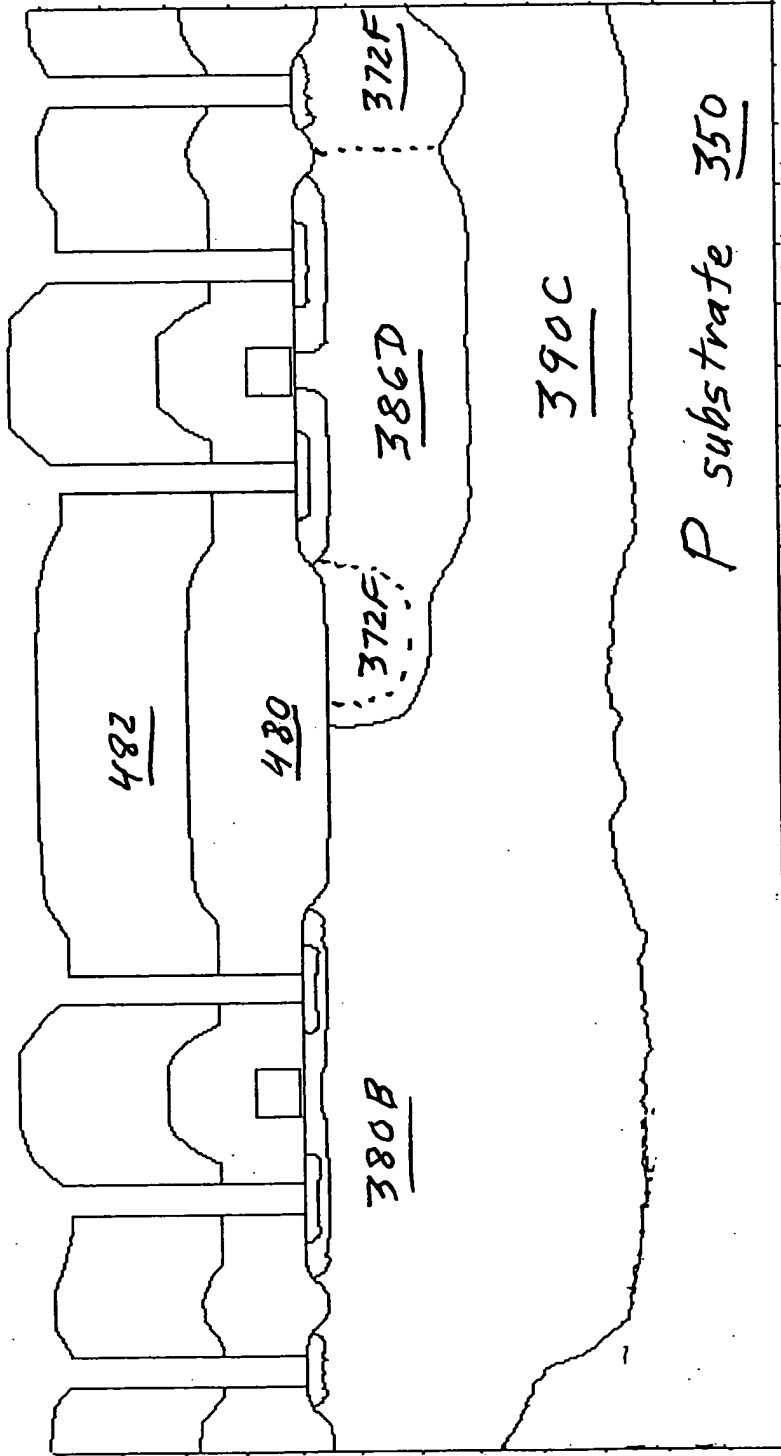
Interlayer Dielectric Deposition and Etch
Fig. 64C

30V Lateral Trench DMOS 308



Interlayer Dielectric Deposition and Etch
Fig. 64D

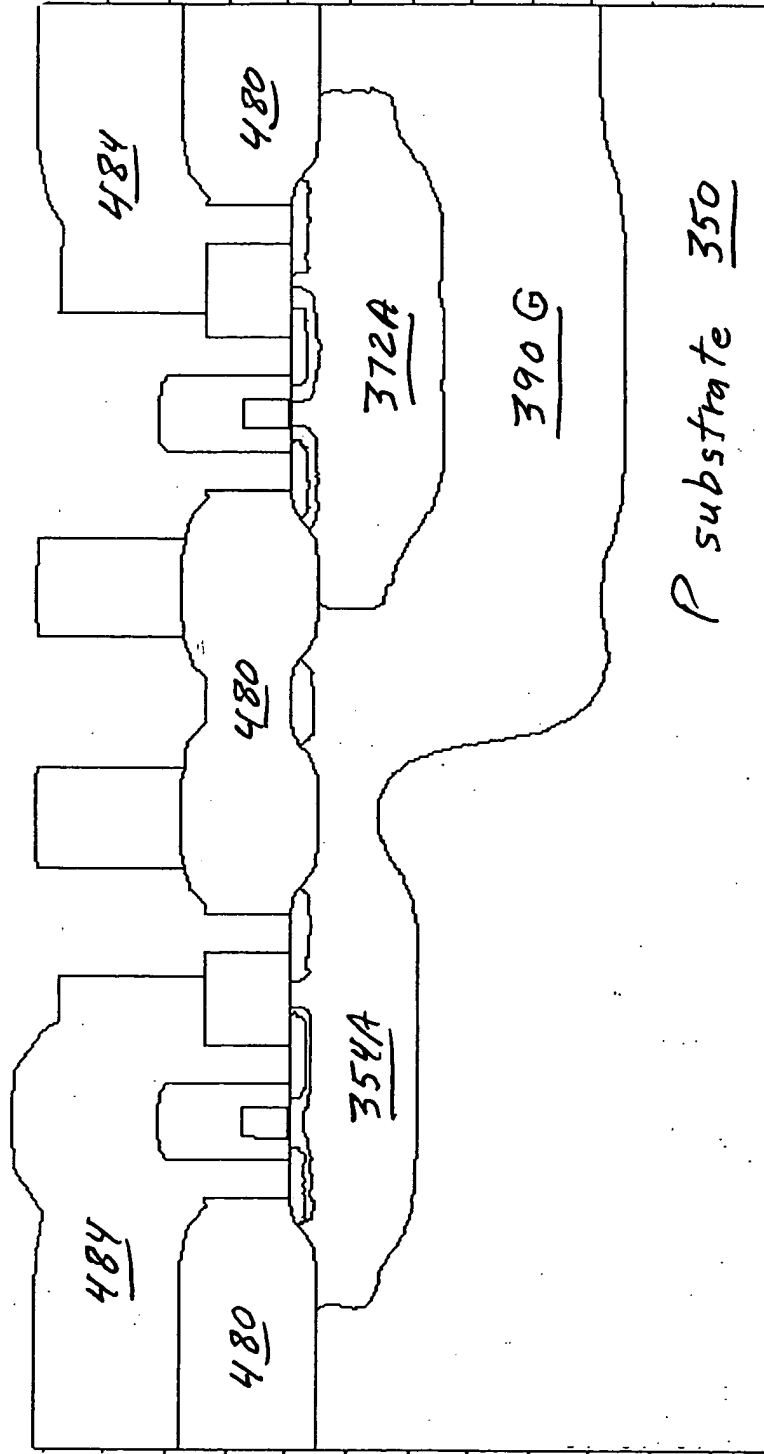
Symmetrical 12V CMOS
 12V PMOS 309 12V NMOS 310



P substrate 350

Interlayer Dielectric Deposition and Etch
Fig 64E

5V PMOS 301 5V NMOS 302

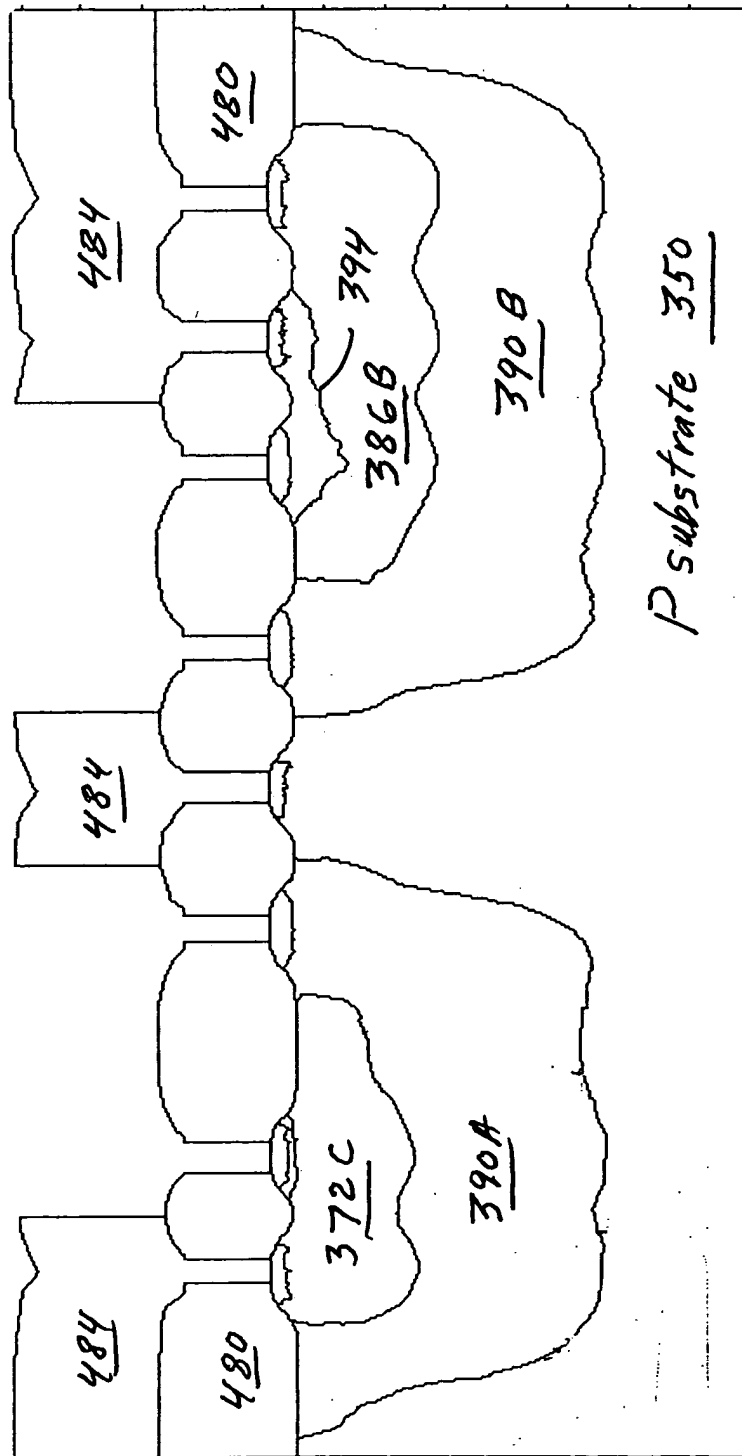


N+plug Mask and Implant
Fig. 65A

High F_T Layout

5V NPN 305

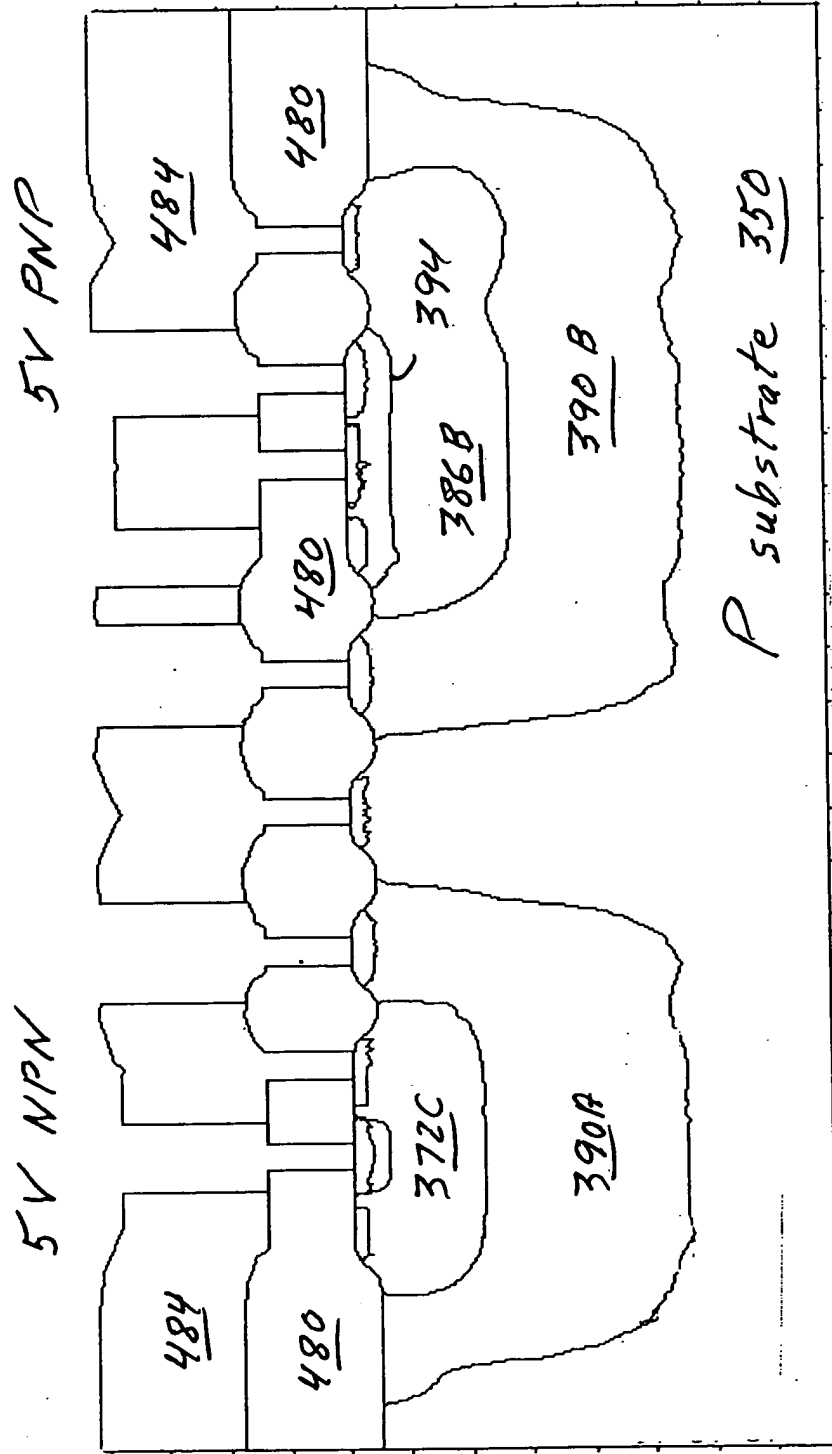
5V PNP 306



N-play Mask and Implant
Fig 6513

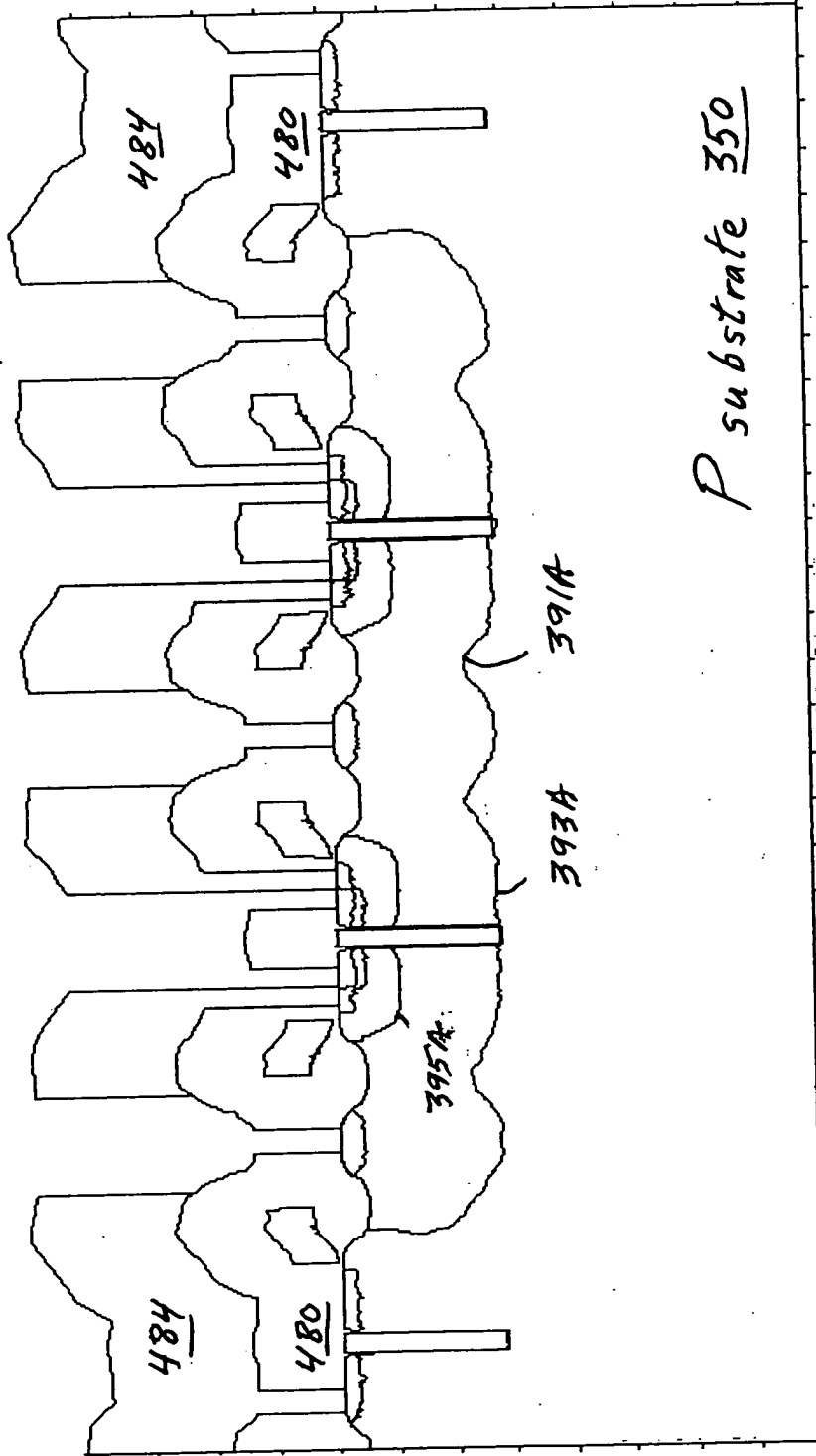
201/219

Conventional Layout



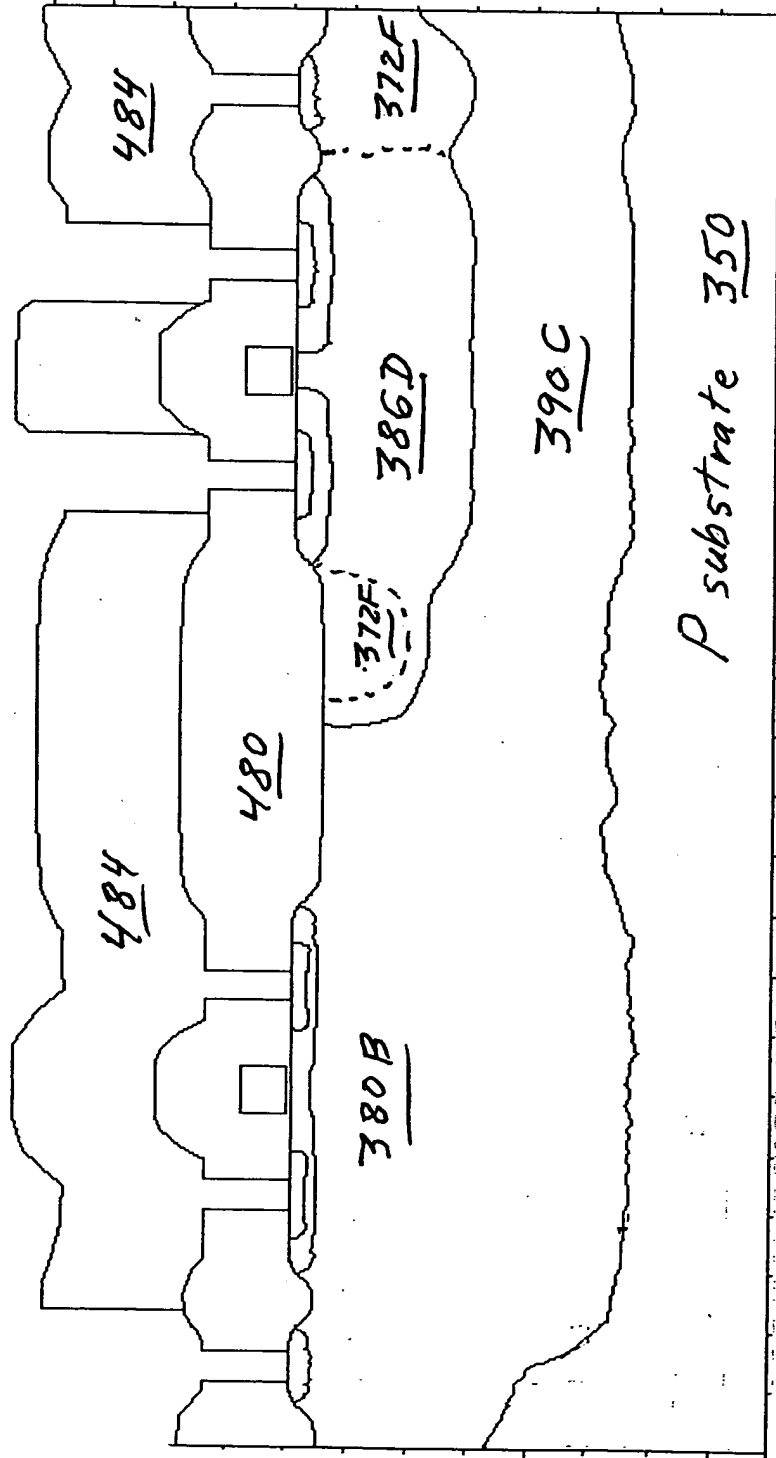
N-plug Mask and Implant
Fig. 65C

30V Lateral Trench DMOS 308



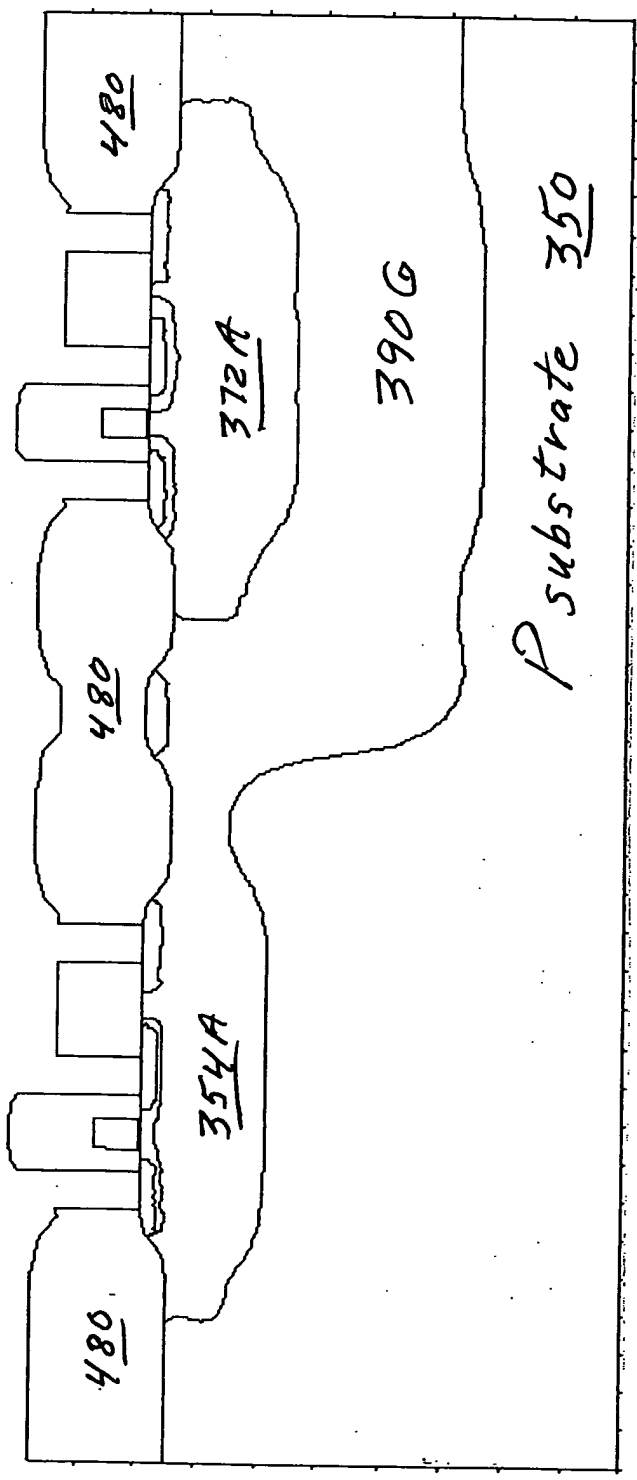
N+poly Mask and Implant
Fig 65D

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



N-plug Mask and Implant
Fig 65E

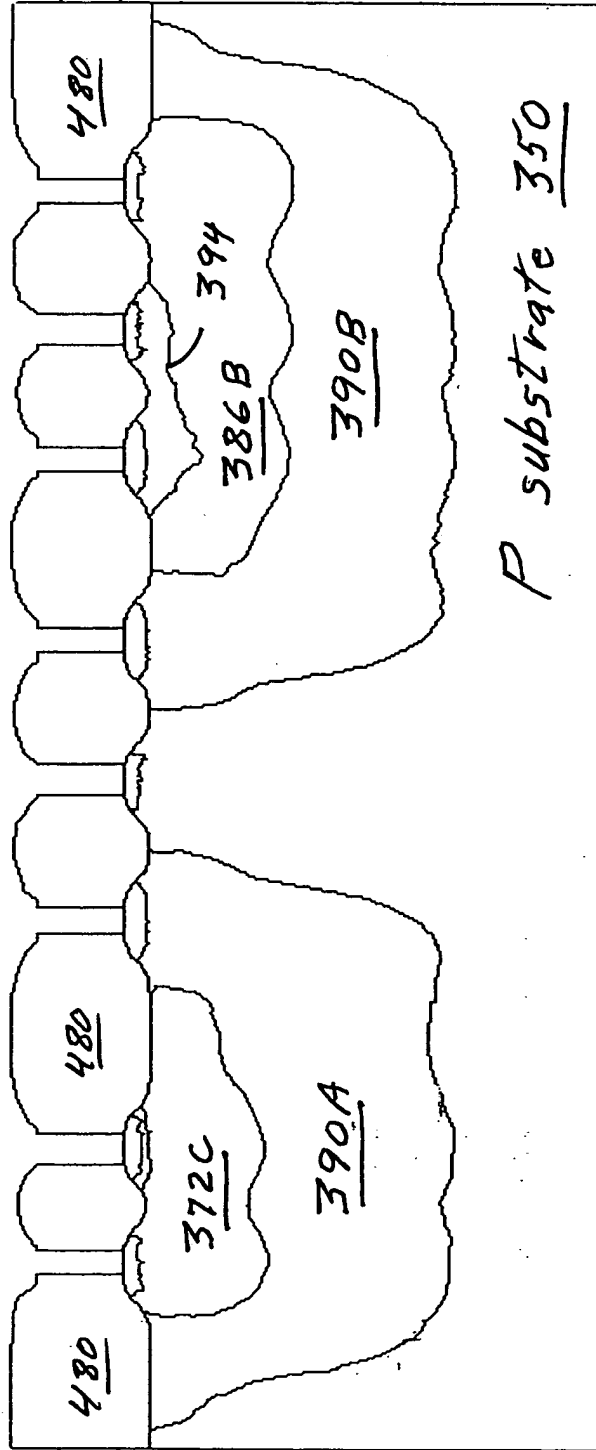
5V PMOS 301 5V NMOS 302



P-plug Implant
Fig. 66A

High F_T Layout

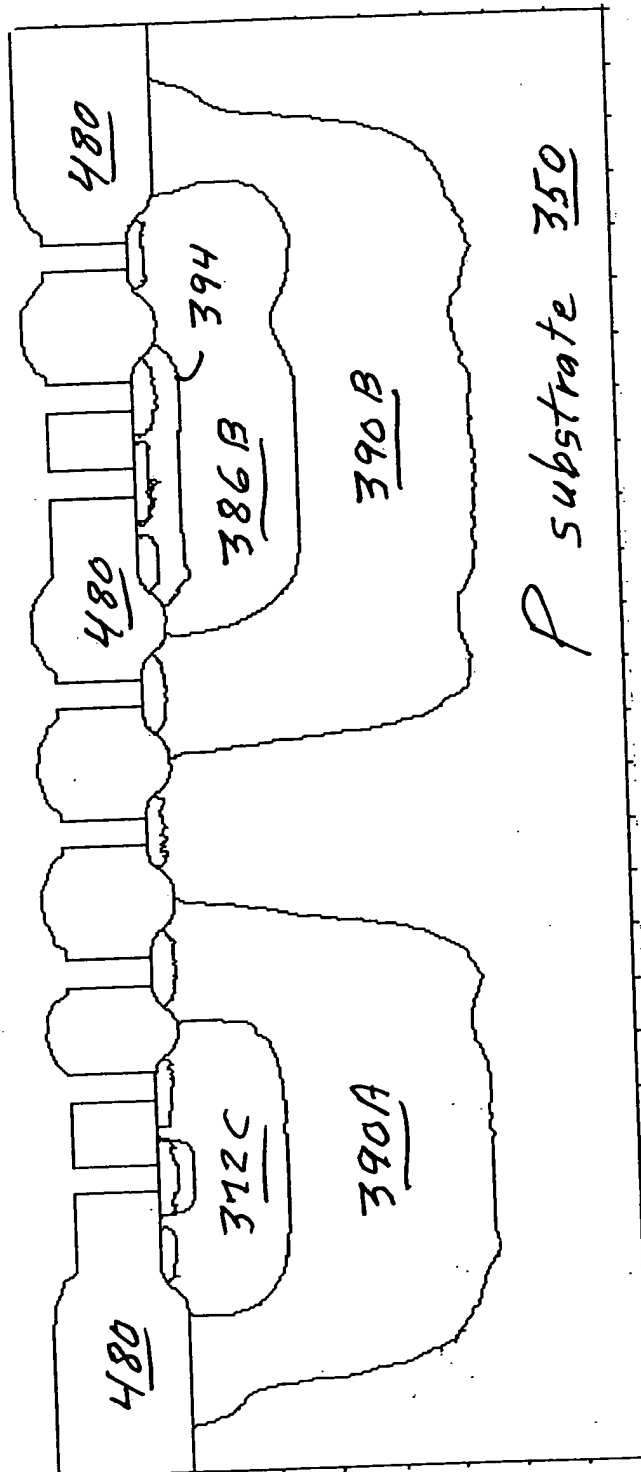
5V NPN 305 5V PNP 306



P-plug Implant
Fig. 66B

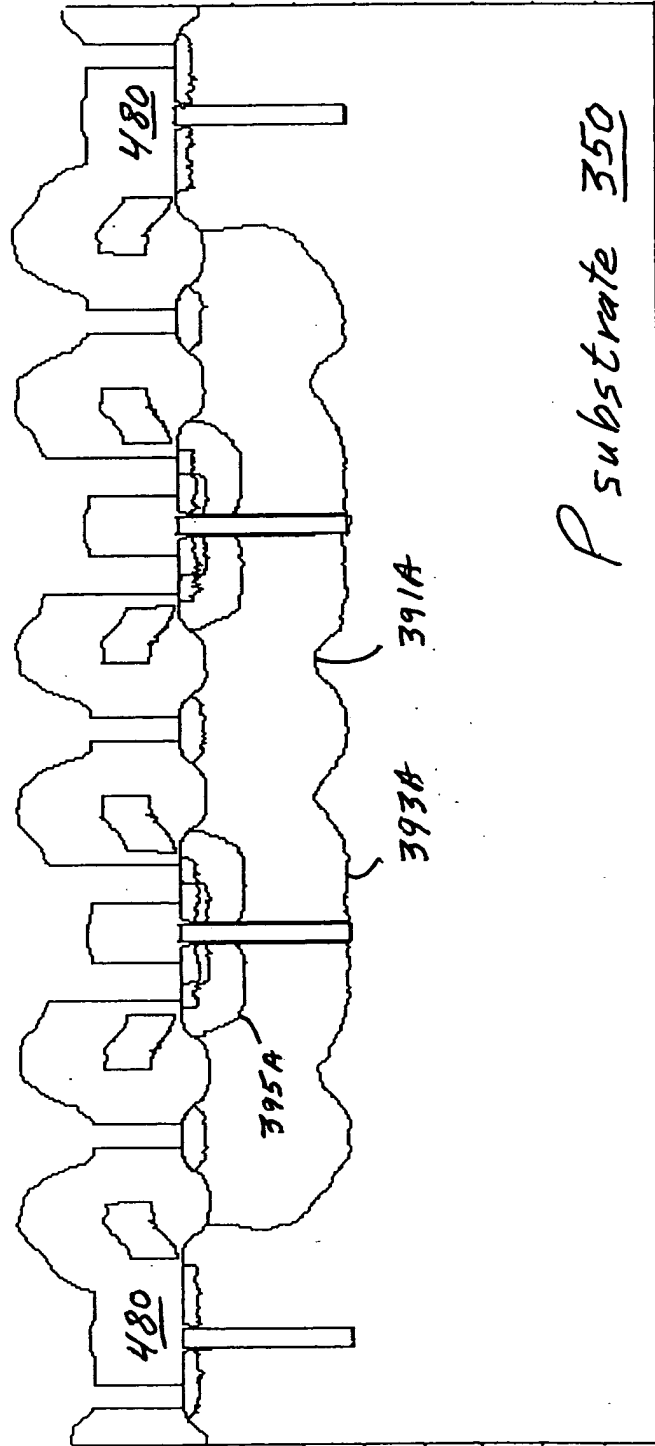
Conventional Layout

5V NPN 5V PNP



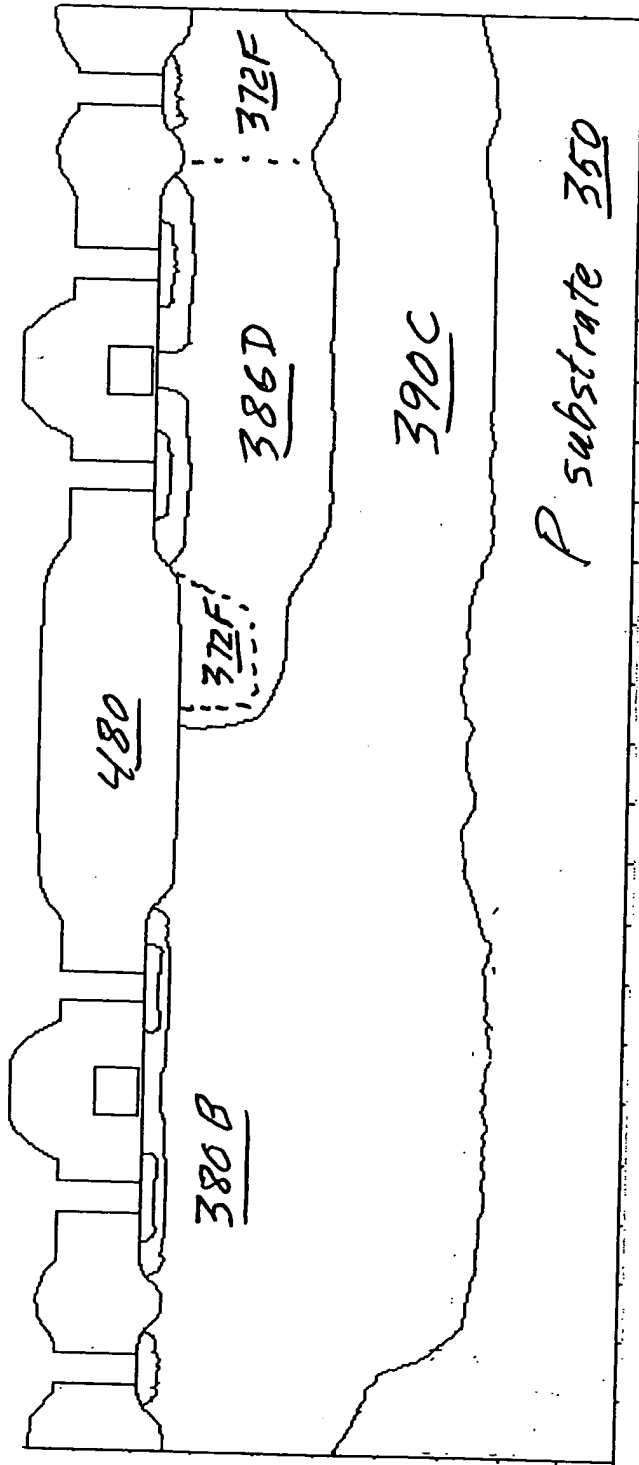
R. P. Iyengar
Fig. 66C

30V Lateral Trench DMOS 308



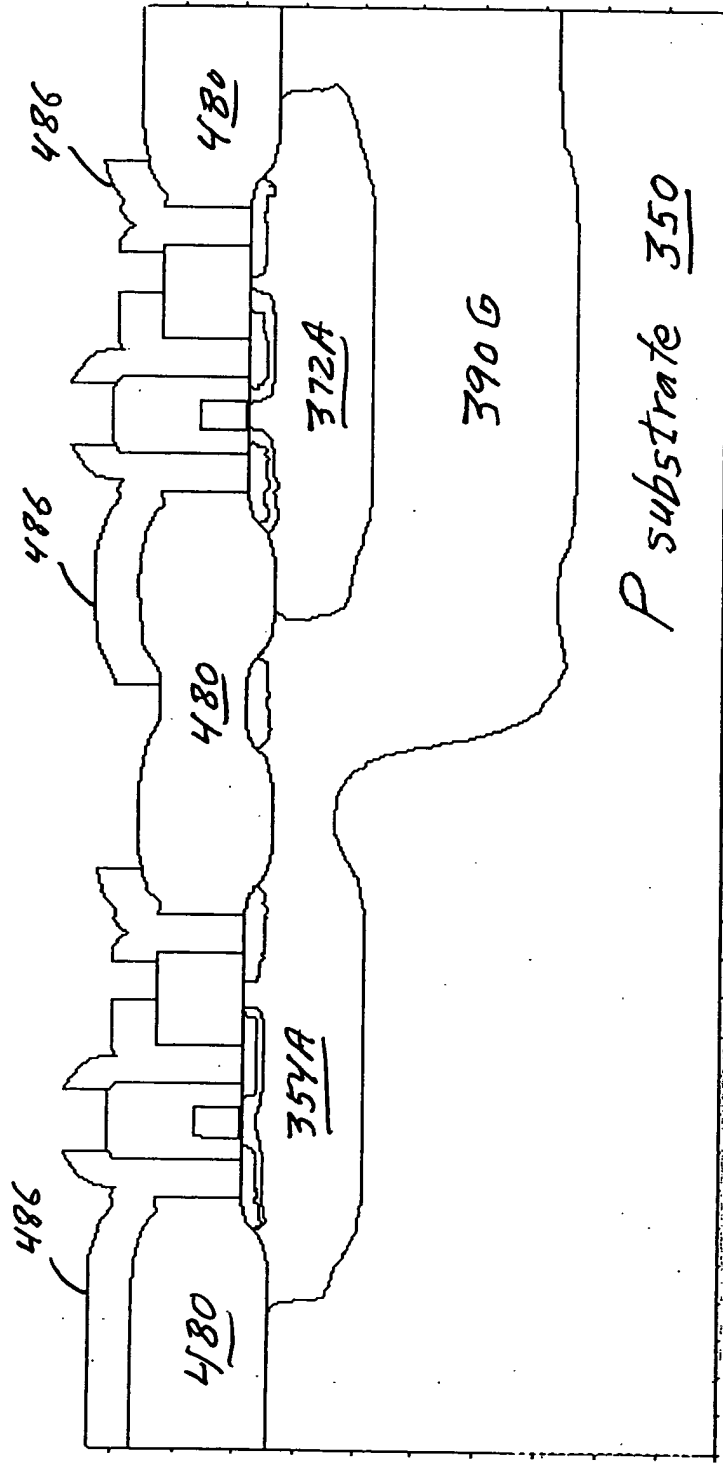
P-plug Implant
Fig 66D

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



P-plug Implant
Fig. 66E

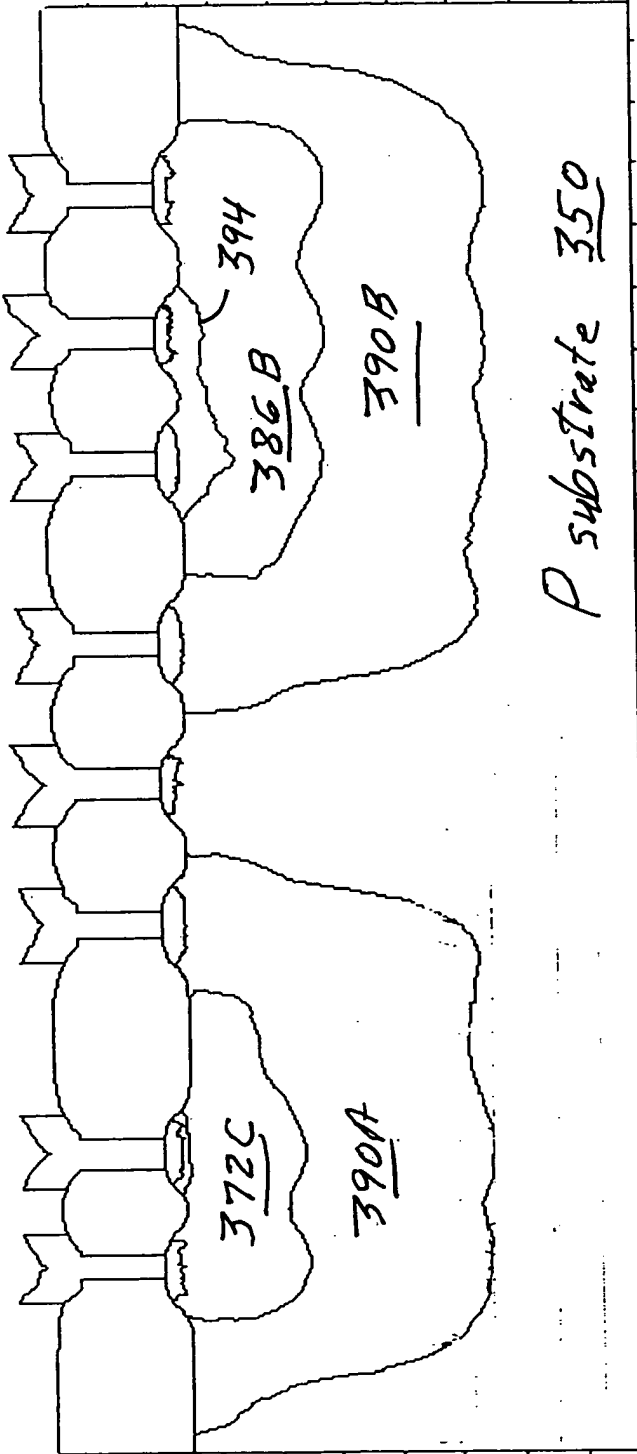
5V PMOS 301 5V NMOS 302



Metal Layer
Fig. 67A

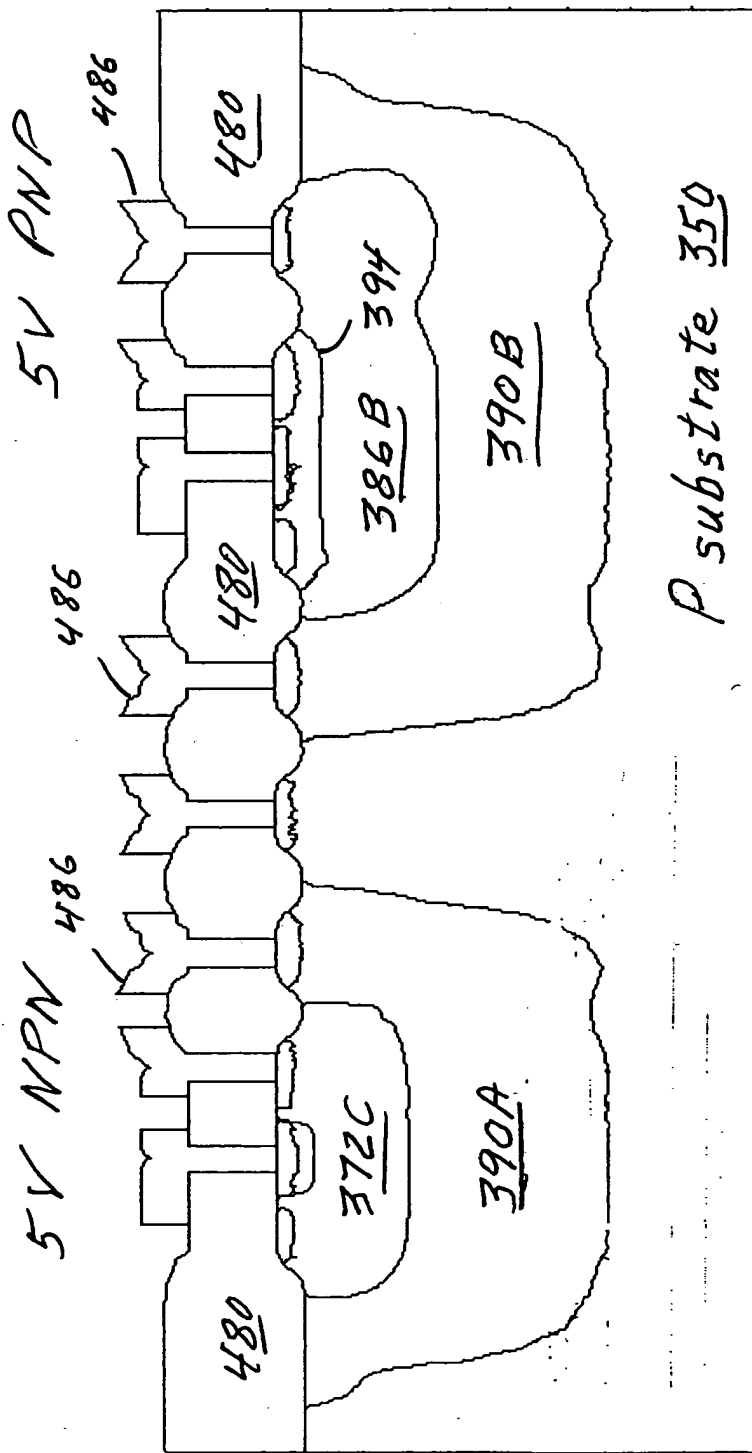
High F_T Layout

5V NPN 305 5V PNP 306



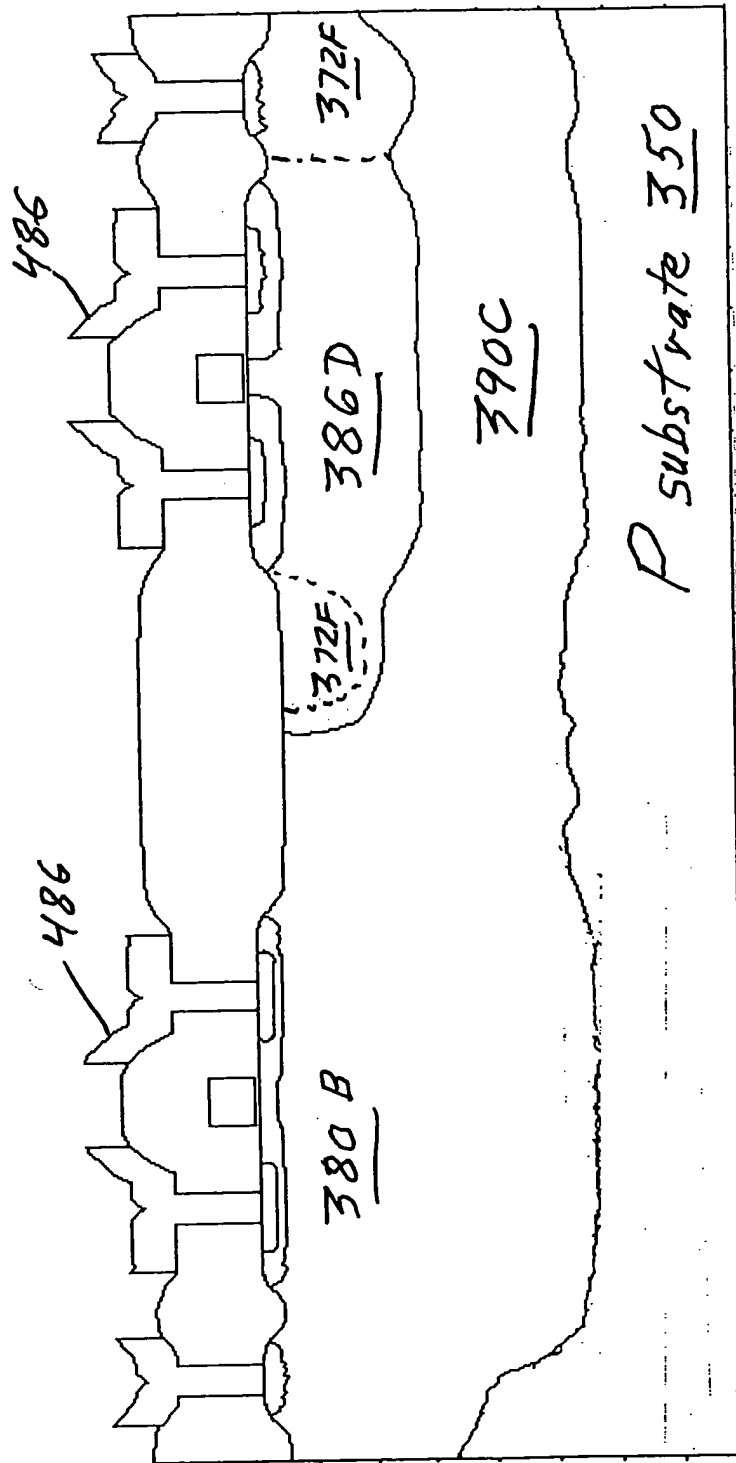
Metal Layer
Fig. 67B

Conventional layout



Metal layer
Fig. 67C

Symmetrical 12V CMOS
12V PMOS 309 12V NMOS 310



Metal Layer
Fig. 67E

Fig. 17V

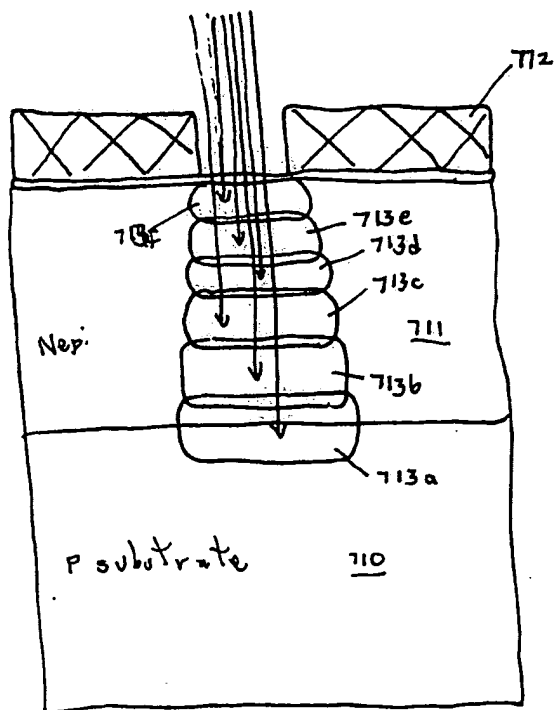


Fig. 17W

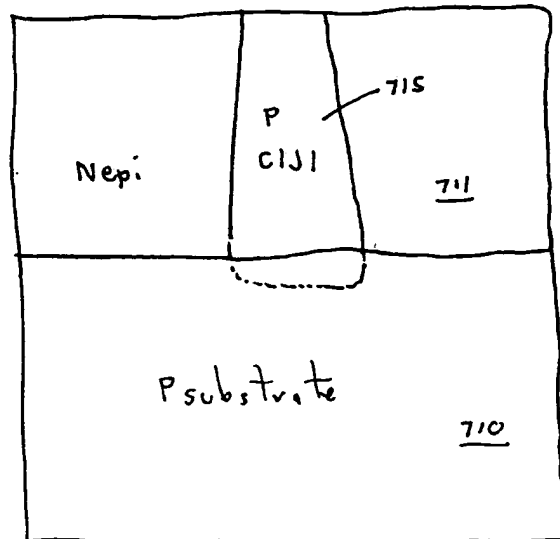


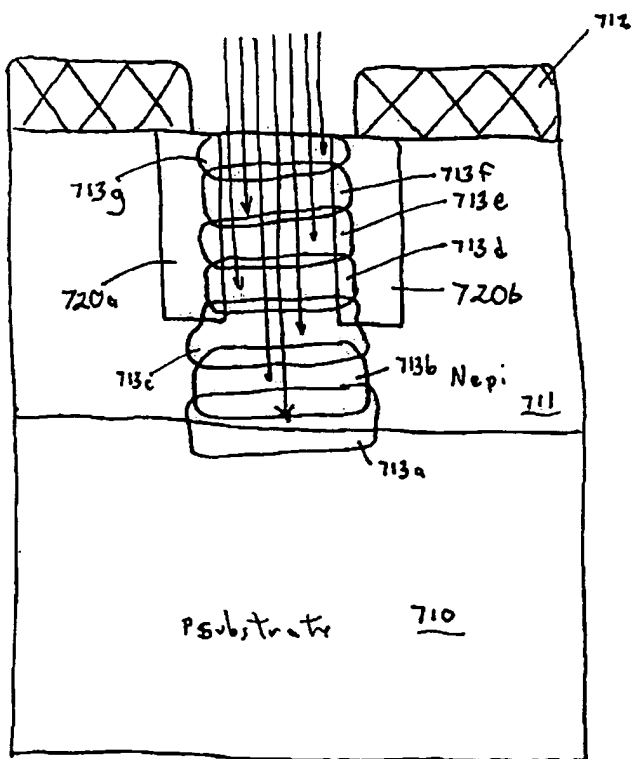
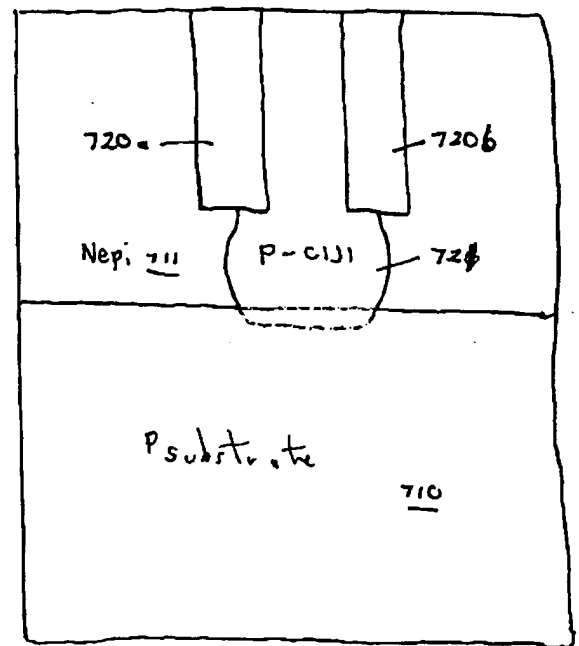
Fig. 17XFig. 17Y

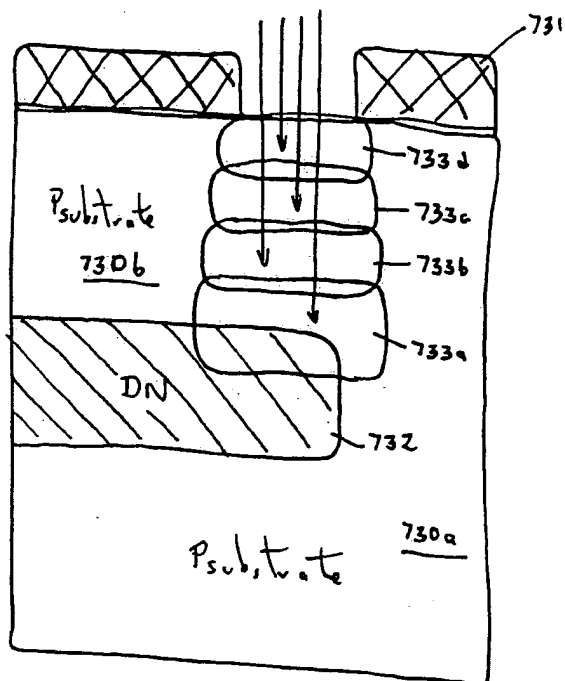
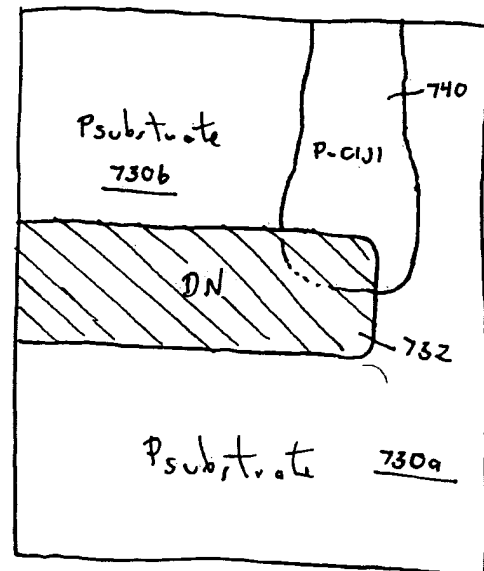
Fig. 17ZFig. 17AA

Fig. 17BB

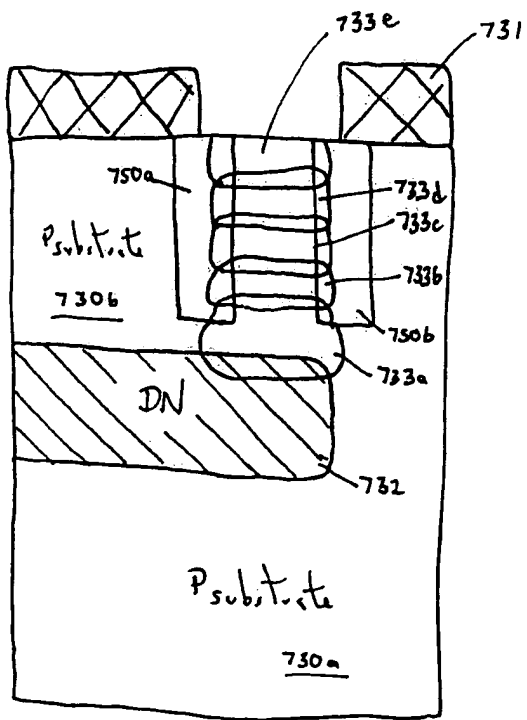


Fig. 17CC

